Service Manual

HP 1652B/1653B
Logic Analyzers

HEWLETT PACKARD
1652B
LOGIC ANALYZER
State Listing
Timing Waveforms
MENU
ROLL
CURSOR
INPUTS

HEWLETT PACKARD

HEWLETT
PACKARD

SERVICE MANUAL

HP 1652B/1653B

Logic Analyzers

SERIAL NUMBERS

This manual applies directly to instruments
prefixed with serial number:

2941A/2942A/3011A/3012A

For Additional Information about serial numbers see
INSTRUMENTS COVERED BY THIS MANUAL
in Section 1.

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CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institute's calibration facility, and to the calibration facilities of other International Standards Organization members.

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This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

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HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument or software, or firmware will be uninterrupted or error free.

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Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW3A789

Safety Considerations

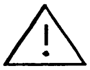
General Operation

This is a Safety Class I instrument (provided with terminal for protective earthing). BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

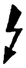
General Warnings and Cautions

- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

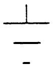
Safety Symbols



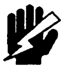
Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.



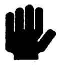
Indicates Hazardous Voltages



Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

Warning 

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

Caution 

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software and/or firmware code may be printed before the date; this indicates the version level of the software and/or firmware of this product at the time of the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1	February 1990	01652-90905

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in Printing History and on the title page.

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General Information

1

Introduction

This Service Manual explains how to test, adjust, and service the Hewlett-Packard 1652B/1653B Logic Analyzer. This manual is divided into six sections:

- 1 - General Information.
- 2 - Installation.
- 3 - Performance Tests.
- 4 - Adjustments and Calibration.
- 5 - Replaceable Parts.
- 6 - Service.

For easier access, the Service section is presented in four sub-sections:

- 6A - Theory of Operation.
- 6B - Self Tests.
- 6C - Troubleshooting.
- 6D - Assembly Removal and Replacement.

Information for operating, programming, and interfacing the HP 1652B/1653B is contained in the HP 1652B/1653B Operating and Programming manual set supplied with each instrument.

Section 1, "General Information," includes a description of the HP 1652B/1653B logic analyzer, including its specifications, options, available accessories, and recommended test equipment for maintaining the instrument.

Listed on the title page of this manual is a microfiche part number. This number can be used to order 4 by 6- inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement and pertinent Service Notes.

Instruments Covered by this Manual

The instrument serial number is located on the rear panel. Hewlett-Packard uses a two part serial number consisting of a four-digit prefix and a five-digit suffix separated by a letter (for example, 0000A00000). The prefix is the same for all identical instruments and changes only when a modification is made that affects parts compatibility. The suffix is assigned and is different for each instrument. This manual applies directly to instruments with the serial prefix shown on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

Safety Considerations

This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before you begin operating this instrument. Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with these precautions, or with specific warnings elsewhere in this manual, violates safety standards of design, manufacture, and intended use of this instrument.

Hewlett-Packard assumes no liability for the customer's failure to comply with these safety requirements.

Product Description

The HP 1652B/1653B logic analyzers are general purpose instruments featuring measurement capabilities in all three domains of interest to the digital system designer: Analog, Timing, and State. Each of these domains is available to the user separately or in an interactive combination.

The HP 1652B includes an 80-channel, 35 MHz state, 100 MHz timing logic analyzer, selectable in 16 channel groupings with a 2-channel, 100 MHz, 400 Msample/s digitizing oscilloscope. The HP 1653B includes an 32-channel, 25 MHz state, 100 MHz timing logic analyzer, also selectable in 16 channel groupings with a 2-channel, 100 MHz, 400 Msample/s digitizing oscilloscope. Both analyzers can be configured as two independent state analyzers or one state and one timing analyzer. Two channels of oscilloscope measurement can be added to any configuration. Some of the main features of the analyzer include the following:

- Simultaneous state/state, or simultaneous state/timing analysis.
- Time interval; number of states; pattern search; minimum, maximum, and average time interval statistics.
- Transitional timing to store data only when there is a transition.
- Clock qualifiers, storage qualification, time and number of state tagging, and prestore.
- Small lightweight probing.

Some of the main features of the digitizing oscilloscope include the following:

- 2 channels of 400 Msamples/s digitizing for 100 MHz bandwidth single-shot analysis.
- 2k memory depth
- Automatic pulse parameters which display time between markers, acquires until capturing specified time between markers, and performs statistical analysis on time between markers.
- Arming by either analyzer or BNC input.
- 60 mV through 40 V full screen resolution.
- Lightweight miniprobes.

Other main features of the HP 1652B/1653B include the following:

- A user interface consisting of a panel keyboard with a Rotary Pulse Generator (RPG) knob.
- Nine-inch white phosphor, high resolution monitor.
- 3.5-inch floppy disk drive.
- HP-IB and RS-232C interfaces for hardcopy output to a printer or controller interface.

Accessories Supplied

The following accessories are supplied with the HP 1652B/1653B Logic Analyzer:

- Woven probe cable (HP part number 01650-61607) with a 40-pin connector on each side, 17 signal lines, 18 return lines, 2 chassis ground lines, and 2 power lines. Each power line supplies +5 volts for preprocessor power. Each cable supplies 600 milliamperes with a maximum power available from the HP 1652B/1653B of 2 amperes. Five probe cables are supplied with the HP 1652B and two are supplied with the HP 1653B.
- Probe Tip Assemblies (HP part number 01650-61608) that provide 16 data channels, 1 clock channel, and 1 ground lead per pod assembly. The probe input specifications are listed in the Logic Analyzer Specifications of this section. Five Probe Tip Assemblies are supplied with the HP 1652B and two are supplied with the HP 1653B.
- Grabbers for the probe tip assemblies are supplied in packages of 20 (HP part number 5959-0288). One-hundred grabbers (5 packages) are supplied with the HP 1652B and 40 grabbers (2 packages) are supplied with the HP 1653B.
- Two HP 10430A 10:1, 1 MΩ, 6.5 pF, 1 m mini-probes.
- Two right angle BNC adapters (HP part number 1250-0076).
- One BNC-to-mini probe adapter (HP part number 1250-1454).
- One Operating System Disk.
- One Performance Verification Disk.
- One 2.3 meter (7.5 feet) Power Cord (see section 2, "Installation," for the available power cords).
- One Operating and Reference Manual Set.
- One Programming Reference Manual.
- One Service Manual.
- One RS-232C Loopback Connector.

Accessories Available

The following accessories are available for the HP 1652B/1653B Logic Analyzer:

- Termination Adapter (HP part number 01650-63201).
- HP Model 10269C General Purpose Probe Interface to connect the logic analyzer directly to microprocessor preprocessors.
- Preprocessors for specific microprocessors and bus systems (for more information see your Hewlett-Packard Sales/Service Offices).
- 10:1, 100:1, 10 MΩ, 10 pf resistive divider probe set, 1.5 m (HP 10020A).
- BNC to BNC cable, 1.2 m (HP 10503A).
- 24-pin IC test clip (HP 10211A).
- BNC-to-BNC ac coupling capacitor (HP 10240B).

10:1 Probes:

  - 1 MΩ, 7.5 pF miniprobe, 1 m (HP 10435A).
  - 1 MΩ, 10 pF miniprobe, 2 m (HP 10433A).

1:1 Probes:

  - 36 pF miniprobe, 1 m (HP 10438A).
  - 62 pF miniprobe, 2 m (HP 10439A).
  - 50 Ω miniprobe, 2 m (HP 10437A).

100:1 Probes:

  - 10 MΩ, 2.5 pF miniprobe, 2 m (HP 10440A).

- Soft Carrying Case (HP part number 1540-1066).
- HP Model 1008A Option 006 Testmobile.
- HP Model 92192A 3.5-inch Microfloppy Disks (box of ten).
- Rackmount Kit (HP part number 5061-6175).

Logic Analyzer Specifications

The following specifications are the performance standards or limits against which the HP 1652B/1653B logic analyzer is tested.

Probes

Minimum Swing: 600 mV peak-to-peak.

Threshold Accuracy:

Voltage Range	Accuracy
-2.0V to +2.0V	± 150 mV
-9.9V to -2.1V	± 300 mV
+2.1V to +9.9V	± 300 mV

State Mode

Clock Repetition Rate: Single phase is 35 MHz maximum (25 MHz on the HP 1653B). With time or state counting, minimum time between states is 60 ns (16.67 MHz). Both mixed and demultiplexed clocking use master-slave clock timing. The master clock must follow the slave clock by at least 10 ns and precede the next slave clock by ≥50 ns.

Clock Pulse Width: ≥10 ns at threshold.

Setup Time: Data must be present prior to the clock transition, ≥10 ns.

Hold Time: Data must be present after the rising clock transition, 0 ns.

Data must be present after the falling clock transition, 0 ns (HP 1653B). Data must be present after the falling L clock transition, 0 ns (HP 1652B). Data must be present after the falling J, K, M, and N clock transition, 1 ns (HP 1652B).

Timing Mode

Minimum Detectable Glitch: 5 ns wide at the threshold.

Logic Analyzer Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP 1652B/1653B logic analyzer. These characteristics are included as additional information for the user.

Probes

Input RC: 100 KΩ ± 2% shunted by approximately 8 pF at the probe tip.

Dynamic Range: ± 10 volts about the threshold.

TTL Threshold Preset: +1.6 volts.

ECL Threshold Preset: -1.3 volts.

Threshold Range: -9.9 to +9.9 volts in 0.1 volt increments.

Threshold Setting: Threshold levels may be defined for pods 1 and 2 individually (HP 1653B). Threshold levels may be defined for pods 1, 2, and 3 on an individual basis and one threshold may be defined for pods 4 and 5 (HP 1652B).

Minimum Input Overdrive: 250 mV or 30% of the input amplitude, whichever is greater.

Maximum Voltage: ± 40 volts peak.

Maximum Power Available Through Cables: 600 mA at 5V per cable; 2 amp @ 5V per HP 1652B/1653B.

Measurement Configurations

Analyzer Configurations:

Analyzer 1	Analyzer 2
Timing	Off
Off	Timing
State	Off
Off	State
Timing	State
State	Timing
State	State
Off	Off

Channel Assignment: Each group of 16 channels (a pod) can be assigned to Analyzer 1, Analyzer 2, or remain unassigned. The HP 1652B contains 5 pods; the HP 1653B contains 2 pods.

State Analysis

Memory

Data Acquisition: 1024 samples/channel.

Trace Specification

Clocks: Five clocks (HP 1652B) or two clocks (HP 1653B) are available and can be used by either one or two state analyzers at any time. Clock edges can be ORed together and operate in single phase, two phase demultiplexing, or two phase mixed mode. The clock edge is selectable as positive, negative, or both edges for each clock.

Clock Qualifier: The high or low level of four ORed clocks (HP 1652B) or one clock (HP1653B) can be ANDed with the clock specification. Setup time: 20 ns; hold time: 5 ns.

Pattern Recognizers: Each recognizer is the AND combination of bit (0, 1, or X) patterns in each label. Eight pattern recognizers are available when one state analyzer is on. Four are available to each analyzer when two state analyzers are on.

Range Recognizers: Recognizes data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones). One range term is available and is assigned to the first state analyzer turned on. The maximum size is 32 bits and on a maximum of 2 pods.

Qualifier: A user-specified term that can be anystate, nostate, a single pattern recognizer, range recognizer, or logical combination of pattern and range recognizers.

Sequence Levels: There are eight levels available to determine the sequence of events required for trigger. The trigger term can occur anywhere in the first seven sequence levels.

Branching: Each sequence level has a branching qualifier. When satisfied, the analyzer will restart the sequence or branch to another sequence level.

Occurrence Counter: Sequence qualifier may be specified to occur up to 65535 times before advancing to the next level.

Storage Qualification: Each sequence level has a storage qualifier that specifies the states that are to be stored.

Enable/Disable: Defines a window of post-trigger storage. States stored in this window can be qualified.

Prestore: Stores two qualified states that precede states that are stored.

Tagging

State Tagging: Counts the number of qualified states between each stored state. A measurement can be shown relative to the previous state or relative to trigger. Maximum count is 4.4 X (10 to the 12th power).

Time Tagging: Measures the time between stored states, relative to either the previous state or to the trigger. Maximum time between states is 48 hours.

With tagging on, the acquisition memory is halved; minimum time between states is 60 ns.

Symbols

Pattern Symbols: A mnemonic can be defined for the specific bit pattern of a label. When the data display is SYMBOL, a mnemonic is displayed where the bit pattern occurs. Bit patterns can include zeros, ones, and don't cares.

Range Symbols: A mnemonic can be defined covering a range of values. Bit pattern for lower and upper limits must be defined as a pattern of zeros and ones. When the data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from the base of the range.

Number of Pattern and Range Symbols: 200 per HP 1652B/1653B.

Symbols can be down-loaded over RS-232C and HP-IB.

State Compare Mode

This mode performs a post-processing bit-by-bit comparison of the acquired state data and the compare data image.

Compare Image: This is created by copying a state acquisition into the compare image buffer. It allows editing of any bit in the compare image to a zero, one, or don't care.

Compare Image Boundaries: Each channel (column) in the compare image can be enabled or disabled via bit masks in the compare image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.

Stop Measurement: Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current compare image is equal or not equal.

Displays: Compare Listing display shows the compare image and bit masks. The Difference Listing display highlights differences between the current state acquisition and the current compare image.

State X-Y Chart Display

This function plots the value of the specified label on the y-axis versus states or another label on the x-axis. Both axes can be scaled by the user.

Markers: The markers are correlated to state listing, state compare, and state waveform displays. They are available as pattern, time, or statistics (with time counting on), and states (with state counting on).

Accumulate: Chart display is not erased between successive acquisitions.

State Waveform Display

This function displays a state acquisition in a waveform format.

States/div: 1 to 104 states.

Delay: -1023 to 1024 states.

Accumulate: The waveform display is not erased between successive acquisitions.

Overlay Mode: Multiple channels can be displayed on one waveform display line. The primary use is to view a summary of bus activity.

Maximum Number of Displayed Waveforms: 24.

Markers: The markers are correlated to state listing, state compare, and X-Y chart displays. The markers can be used for pattern, time, or statistics (with time counting on), and states (with state counting on).

Timing Analysis

Transitional Timing Mode

A sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of a waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.

Sample Period: 10 ns.

Maximum Time Covered By Data: 5,000 seconds.

Minimum Time Covered by Data: 10.24 μs.

Glitch Capture Mode

Data sample and glitch information is stored every sample period.

Sample Period: 20 ns to 50 ms in a 1-2-5 sequence dependent on seconds/division and delay settings.

Memory Depth: 512 samples/channel.

Time Covered by Data: Sample period X 512.

Waveform Display

Sec/div: 10 ns to 100 s; 0.01% resolution.

Screen Delay: -2500 s to 2500 s. The presence of data is dependent on the number of transitions in data between the trigger and trigger plus delay (transitional timing).

Accumulate: The waveform display is not erased between successive acquisitions.

Hardware Delay: ±(20 ns to 10 ms).

Overlay Mode: Multiple channels can be displayed on one waveform display line. The primary use is to view a summary of bus activity.

Maximum Number Of Displayed Waveforms: 24.

Time Interval Accuracy

Channel to Channel Skew: 4 ns typical.

Sample Period Accuracy: 0.01% of sample period.

Time Interval Accuracy: ± (sample period + channel-to-channel skew + 0.01% of time interval reading).

Trigger Specification

Asynchronous Pattern: Trigger on an asynchronous pattern less than or greater than a specified duration. The pattern is the logical AND of a specified low, high, or don't care for each assigned channel. If the pattern is valid but the duration is invalid, there is a 20 ns reset time before the instrument will look for patterns again.

Greater Than Duration: Minimum duration is 30 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Accuracy is +0 ns to -20 ns. Trigger occurs at pattern + duration.

Less Than Duration: Maximum duration is 40 ns to 10 ms with 10 ns or 0.01% resolution, whichever is greater. Pattern must be valid for at least 20 ns. Accuracy is +20 ns to -0 ns. Trigger occurs at the end of the pattern.

Glitch/Edge Triggering: Trigger on a glitch or edge following a valid duration of an asynchronous pattern while the pattern is still present. Edge can be specified as rising, falling, or either. Less than duration forces glitch and edge triggering off.

Measurement and Display Functions

Autoscale (Timing Analyzer Only)

Autoscale searches for and displays channels with activity on the pods assigned to the timing analyzer.

Acquisition Specifications

Arming: Each analyzer can be armed by the run key, the other analyzer, the oscilloscope, or the external trigger in port.

Trace Mode: Single mode acquires data once per trace specification. Repetitive mode repeats single mode acquisitions until stop is pressed or until the time interval between two specified patterns is less than or greater than a specified value, or within or not within a specified range. There is only one trace mode when two analyzers are on.

Labels

Channels may be grouped together and given up to a six character name. Up to 20 labels in each analyzer may be assigned with up to 32 channels per label. The primary use is for naming groups of channels such as address, data, and control busses.

Indicators

Activity Indicators: Provided in the Configuration, State Format, and Timing Format menus for identifying high, low, or changing states on the inputs.

Markers: Two markers (X and 0) are shown as dashed lines on the display.

Trigger: The trigger is displayed as a vertical dashed line in the timing waveform display and as line 0 in the state listing display.

Marker Functions

Time Interval: The X and 0 markers measure the time interval between one point on a timing waveform and trigger, two points on the same timing waveform, two points on different waveforms, or two states (time tagging on).

Delta States (State Analyzer Only): The X and 0 markers measure the number of tagged states between one state and trigger, or between two states.

Patterns: The X and 0 markers can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The 0 marker can also find the nth occurrence of a pattern before or after the X marker.

Statistics: The X to 0 marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum X to 0 time, maximum X to 0 time, average X to 0 time, and ratio of valid runs to total runs.

Run/Stop Functions

Run: Starts the acquisition of data in a specified trace mode.

Stop: In single trace mode or the first run of a repetitive acquisition, STOP halts the acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, STOP halts the acquisition of data and does not change current display.

Data Display/Entry

Display Modes: State listing; timing waveforms; interleaved, time-correlated listing of two state analyzers (time tagging on); time-correlated state listing and timing waveform display (state listing in upper half, timing waveform in lower half, and time tagging on).

Timing Waveform: Pattern readout of timing waveforms at X or 0 marker.

Bases: Binary, Octal, Decimal, Hexadecimal, ASCII (display only), and User-defined symbols.

Oscilloscope Specifications

The following specifications are the performance standards or limits against which the oscilloscope in the HP 1652B/1653B is tested.

Vertical

Bandwidth (-3 dB): dc to 100 MHz (single shot).

DC Gain Accuracy: ± 3% of full scale.

DC Offset Accuracy: ± (2 mV + 2% of the channel offset + 2.5% of full scale).

Voltage Measurement Accuracy (DC): (Gain accuracy + ADC resolution + Offset accuracy).

Horizontal

Time Interval Measurement Accuracy: ±(2% X s/div + 0.01% X delta-t + 500 ps).

Trigger

Sensitivity: 10% of full screen.

Oscilloscope Operating Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the oscilloscope in the HP 1652B/1653B. These are included as additional information for the user.

Vertical (at BNC)

Transition Time (10% to 90%): ≤ 3.5 ns.

Number of Channels: 2.

Vertical Sensitivity Range: 15 mV/div to 10 V/div (1:1 probe).

Vertical Sensitivity Resolution: Adjustable 2 digit resolution.

Maximum Sample Rate: 400 MSamples/second.

Analog-to-Digital Conversion: 6 bit real-time.

Analog-to-Digital Resolution: ±1.6% of full scale.

Waveform Record Length: 2048 points.

Input R: 1 MΩ ± 1% or 50 Ω ± 1%.

Input C: Approximately 7 pF.

Input Coupling: dc.

Maximum Safe Input Voltage:

1 MΩ input	± 250 V [dc + peak ac (< 10 kHz)]
50 Ω input	± 5 V RMS

DC Offset Range (1:1 Probe):

Vertical Sensitivity	Available Offset
≤50 mV/div	±2.0 V
100 mV/div - 200 mV/div	±10 V
500 mV/div - 1 V/div	±50 V
≥2 V/div	±125 V

±5 V max if input impedance is at 50 Ω.

DC Offset Resolution (1:1 Probe):

Vertical Sensitivity	Resolution
≤50 mV/div	200 μV
100 mV/div - 200 mV/div	1 mV
500 mV/div - 1 V/div	5 mV
≥2 V/div	25 mV or 4 digits of resolution, whichever is greater

Probe Factors: Any integer ratio from 1:1 to 1000:1.

Channel Isolation: 40 dB: dc to 50 MHz.

30 dB: 50 MHz to 100 MHz (with channels at equal sensitivity).

Horizontal

Timebase Range: 5 ns/div to 5 s/div.

Timebase Resolution:

Time/Division Setting	Resolution
t < 10 ns/div	100 ps
t≥10 ns/div	adjustable with 3-digit resolution

Delay Pre-trigger Range:

Time/Division Setting	Delay
5 ns ≤ s/div ≤ 500 ns	5 X (sec/div)
500 ns ≤ s/div ≤ 5 s	2.5 μs

Delay Post-trigger Range:

Time/Division Setting	Available Delay
25 ms - 5 s/div	40 X (s/div)
100 μs - 25 ms/div	1 s
5 ns - 100 μs/div	10,000 X (s/div)

Trigger

Triggering on either input channel, rising or falling edge.

Trigger Level Range: dc Offset ±5 divisions.

Trigger Level Resolution (1:1 Probe):

Trigger Level	Resolution
≤50 mV/div	400 μV
100 mV/ div - 200 mV/div	2 mV
500 mV/div - 1 V/div	10 mV
≥2 V/div	50 mV

Arming: Armed by the Run key, external BNC low input, or by Analyzer 1 or 2.

Trigger Modes

Immediate: Triggers immediately after the arming condition is met.

Edge: Triggers on the rising or falling edge from channel 1 or 2.

Auto-Trigger: Self-triggers if no trigger condition is found within approximately 1 second after arming.

Trigger Out: Arms Analyzer 1 or 2, or triggers the rear panel BNC.

Waveform Display

Display Formats: 1 to 8 oscilloscope waveforms can be displayed.

Display Resolution: 500 points horizontally, 240 points vertically.

Display Modes

Normal: New acquisitions replace old acquisitions on screen.

Accumulate: New acquisitions are added to the screen and displayed with the previous acquisitions until a parameter is changed and a new acquisition is made.

Average: New acquisitions are averaged with older acquisitions and displayed. The maximum number of averages is 256.

Overlay: Channels 1 and 2 can be overlayed in the same display area.

Connect-the-dots: Provides a display of the sample points which are connected by straight lines.

Waveform Reconstruction: A reconstruction filter fills in the missing data points when the timebase is set to ≤100 ns/division or when the timebase setting is reduced to a point where there are fewer than 500 data samples on the screen.

Waveform Math: Display capability of A-B, B-A, and A + B functions is provided.

Mixed Mode: Oscilloscope plus logic analyzer displays on the same screen.

Measurement Aids

Time Markers: Two vertical markers labeled X and O. Voltage levels are displayed for each marker. Time interval measurements can be made between any two events.

Automatic Search: Searches for a specified absolute or percentage voltage level at a positive or negative edge with count adjustable from 1 to 1024.

Auto Search Statistics: Displays mean, maximum, and minimum values for elapsed time from X to O markers for multiple runs. The number of valid runs and total number of runs are also displayed.

Trigger Level Marker: A horizontal trigger level marker is displayed in the Trace/Trigger menu only.

Automatic Measurements: The following pulse parameter measurements can be performed automatically:

Frequency
Period
V p-p
Rise time
Fall time
Preshoot
Overshoot
+ pulse width
- pulse width

Grid: Selectable (On/Off).

Setup Aids

Autoscale: Automatically sets the vertical and horizontal ranges, offset, and trigger levels to display the input signals. This requires an amplitude above 10 mV peak, and a frequency between 50 Hz and 100 MHz.

Preset: Scales the vertical range, offset, and trigger level to predetermined values for displaying ECL or TTL waveforms.

Preset	Vertical Range	Offset	Trigger Level
TTL*	1.5 V	2.5 V	1.60 V
ECL*	500 mV	-1.3 V	-1.3 V

* Values when Probe = 10:1.

Calibration: Offset, attenuation, gain, trigger level, delay, and set to defaults.

Probe Compensation Source: The external BNC supplies a square wave signal of approximately -400 mV to -900 mV at approximately 1.25 kHz.

Interactive Measurements

Acquisition

Oscilloscope, timing, and state can occur simultaneously or in series.

Mixed Displays

Timing channels and oscilloscope channels can be displayed on the same screen. Multiple state machine listings can be displayed with time tags on the same screen. Timing channels can be displayed with a state listing with Time Tags turned on. State listings with time tags, timing channels, and oscilloscope channels can be displayed on the same screen.

Time Correlation

All modules are time correlated with the exception of when the oscilloscope is being armed by the logic analyzer, and when the oscilloscope is not in trigger immediate mode.

Time Interval Accuracy between Modules

Equals the sum of channel to channel time interval accuracies of each machine used for a measurement.

General Characteristics

The following general characteristics for the HP 1652B/1653B include the environment operating conditions, shipping weights, and instrument dimensions.

Operating Environment

Temperature

Instrument: **Operating:** 0°C to +55°C (32°F to +131°F).
Non-operating: -40°C to +70°C (-40°F to +158°F).

Probes and Cables: 0°C to 65°C (+32°F to +149°F).

Disk Media: 10°C to 50°C (+50°F to +149°F).

Humidity

Instrument: **Operating:** Up to 95% relative humidity (non-condensing) at +40°C (+104°F).
Non-operating: Up to 90% relative humidity at +65°C (+149°F).

Disk Media: 8% to 80% relative humidity at +40°C (+104°F).

Altitude

Operating: Up to 4600 meters (15,000 ft).
Non-operating: Up to 15,300 meters (50,000 ft).

Vibration

Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, 0.3 g (rms)
Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, 2.41 g (rms); Resonant search 5 to 500 Hz swept sine, 1 Octave/minute sweep rate, 0.75 g (0-peak), 5 minute resonant dwell at 4 resonances per axis.

Power Requirements

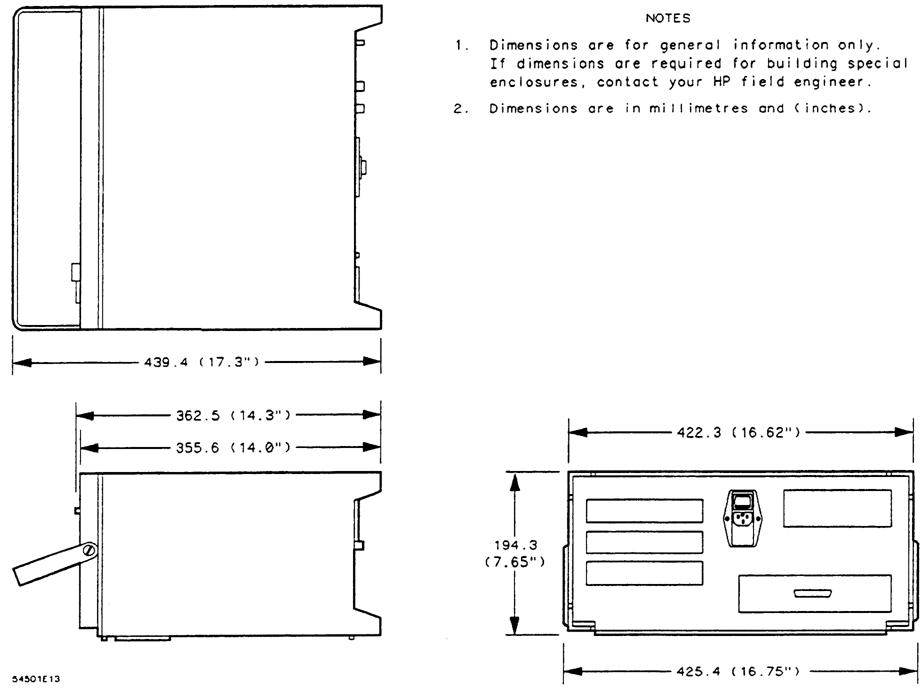
115/230 Vac, -25% to +15%, 48 to 66 Hz, 200 W max.

Weight

10.0 kg (22 lbs) net weight; 18.6 kg (41 lbs) shipping weight.

Dimensions

Refer to the outline drawing below.



NOTES

1. Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer.
2. Dimensions are in millimetres and (inches).

Figure 1-1. HP 1652B/1653B Dimensions

Recommended Test Equipment

Table 1-1 lists the test equipment required to test performance, make adjustments, and troubleshoot the HP 1652B/1653B Logic Analyzer. The table includes the critical specifications of the test equipment and lists each procedure in which the equipment is required. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Recommended Test Equipment

Instrument	Critical Specifications	Recommended Model	Use*
Oscilloscope	dual channel dc to 300 MHz	HP 54502A	P
Pulse Generator	5 ns pulse width 20 ns period 1.3 ns risetime double pulse 100 kHz Repetition Rate Overshoot: 5% of Amp.	HP 8161A/020	P
Pulse Generator	Risetime ≤300 ps	Picosecond Pulse Labs 2700C	A
Signal Generator	Frequency: 100 kHz to 300 MHz Output Accuracy: ±1 dB	HP 8656B	P
Power Supply	±10.2 V output current: 0 to 0.4 amperes	HP 6216C	P
DC Power Supply	Range: ±100 mV to ±5 V Accuracy: ±0.1%	HP 6114A	P, A
Digital Voltmeter	5.5 digit resolution Accuracy: ±0.025%	HP 3478A	P, A, T
Power Meter/ Power Sensor	1 to 500 MHz, -70 dBm to 0 dBm, ±1.2%	HP 436A/ HP 8482A	P
Power Splitter	50 ohms type N, outputs differ by < 0.15 dB	HP 11667A	P
Adapter	Type N male to BNC female (qty. 2)	HP Part Number 1250-0780	P

* P = Performance Tests A = Adjustments T = Troubleshooting

Table 1-1. Recommended Test Equipment (Continued)

Instrument	Critical Specifications	Recommended Model	Use*
Adapter	Type N male to BNC male	HP Part Number 1250-0082	P
Adapter	BNC(female)-to-Dual Banana	HP Part Number 1251-2277	P, A
Adapter	50 ohm feedthrough (Qty 2)	HP 10100C	P
Power Supply Cable	No Substitute	54503-61604	A
BNC Cable	(male-to-male) 48-inch (Qty 2)	HP 10503A	P, A
Cable	Banana (male)-to-Banana (male) (Qty 2)	HP 11000-60001	P, A
Cable	Type N (male) 24-inch	HP 11500B	P
BNC Tee	1M,2F (Qty 2)	HP Part Number 1250-0781	P
Coupler	BNC male-to-male (Qty 2)	HP 1250-0216	P
Resistor	2 Ohms, 25 Watts	HP Part Number 0811-1390	T

* P = Performance Tests A = Adjustments T = Troubleshooting

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2

Installation

Introduction

This section of the manual contains information and instructions necessary for setting up the HP 1652B/1653B Logic Analyzer. This includes inspection procedures, power requirements, hardware connections and configurations, and packaging information.

Safety Considerations

The safety symbols used with Hewlett-Packard instruments are illustrated in the front of this manual. WARNING and CAUTION symbols and instructions should be reviewed before operating the instrument. These warnings and cautions must be followed for your own protection and to avoid damaging the instrument.

Initial Inspection

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, keep it until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment are listed under "Accessories Supplied" in Section 1. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not operate properly, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

Operating Disk Installation

The instrument is shipped with a yellow protective disk in the disk drive. Before applying power to the instrument, remove the protective disk from the disk drive and install the operating system disk. Reinstall the protective disk whenever the instrument is to be transported.

Power Requirements

The HP 1652B/1653B Logic Analyzer requires a power source of either 115 Vac or 230 Vac, -22% to +10%, single phase, 48 to 66 Hz, 200 Watts maximum power.

Caution

BEFORE CONNECTING POWER TO THIS INSTRUMENT, be sure the Line Voltage Select switch on the rear panel of the instrument is set properly and the correct fuse is installed.

Line Voltage Selection

When shipped from the factory, the line voltage selector is set and an appropriate fuse is installed for operating the instrument in the country of destination.

To operate the instrument from a power source other than the one set at the factory:

1. Turn the rear power switch to the OFF position and remove the power cord from the instrument.
2. Remove the fuse module by carefully prying at the top center of the module until you can grasp it and pull it out by hand (see figure 2-1).

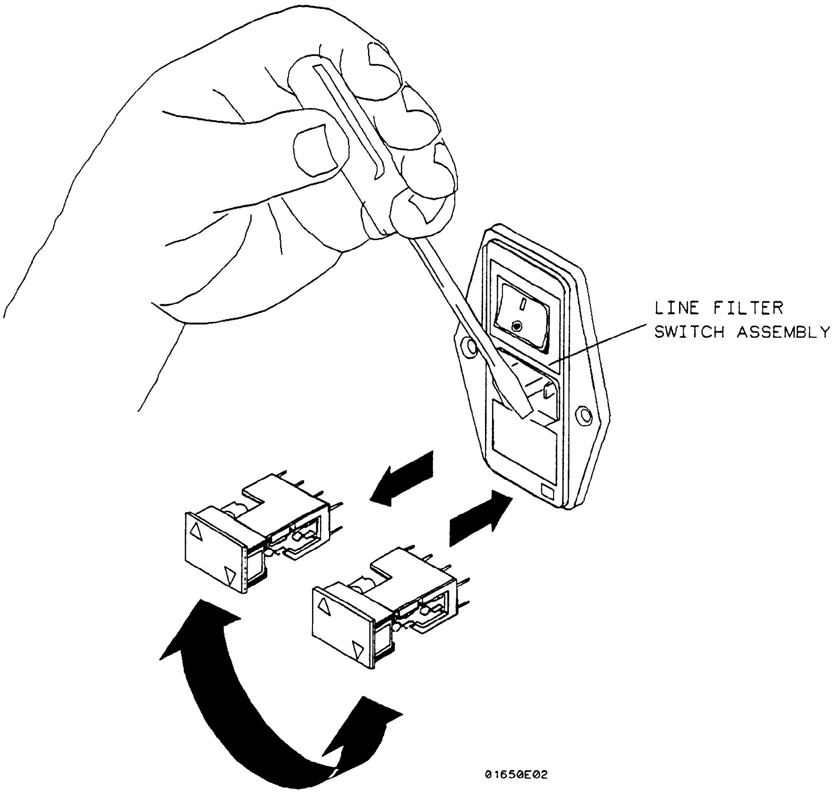


Figure 2-1. Removing the Fuse Module

3. Reinsert the fuse module with the arrow for the appropriate line voltage aligned with the bar on the line filter assembly switch (see figure 2-2).

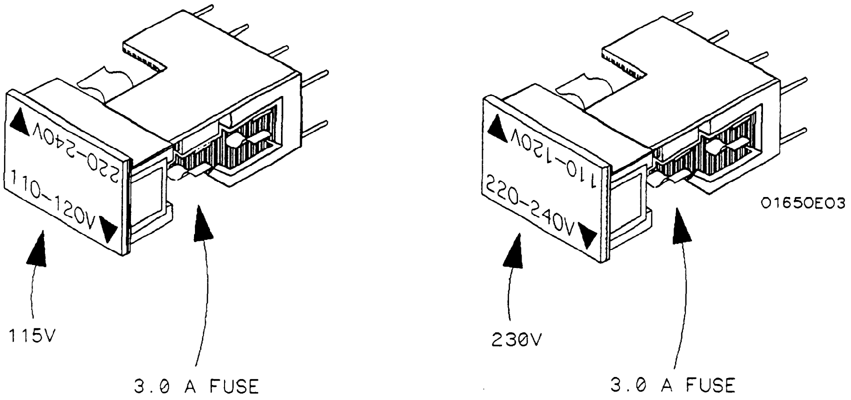


Figure 2-2. Fuse Module Settings

4. Reconnect the power cord, turn the rear power switch to the ON position, and continue normal operation.

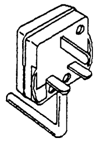
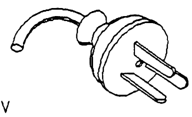
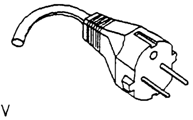
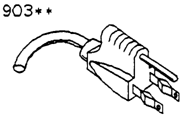
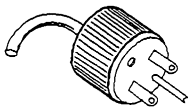
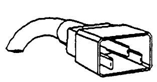
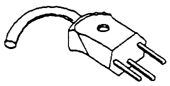
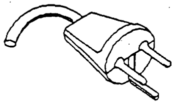
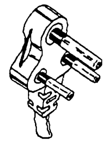
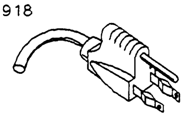
Power Cable

This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See Table 2-1 for the option numbers of available power cables and plug configurations.

Applying Power

When power is applied to the HP 1652B/1653B, a power-up self test is automatically performed. For information on the power-up self test, refer to section 3.

Table 2-1. Power Plug Cord Configurations

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 900  250V	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe, Singapore
OPT 901  250V	8120-1369 8120-0696	Straight *NZSS198/ASC 90°	79/200 87/221	Gray Mint Gray	Australia New Zealand
OPT 902  250V	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So. Africa, India (Unpolarized in many nations)
OPT 903**  125V	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical) UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Mexico, Phillipines, Taiwan
OPT 904**  250V	8120-0698	Straight *NEMA6-15P	90/228	Black	United States, Canada
OPT 905  250V	8120-1396 8120-1625	CEE22-V1 (System Cabinet Use) 250V	30/76 96/244	Jade Gray	For interconnecting system components and peripherals. United States and Canada only
OPT 906  250V	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 912  220V	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark
OPT 917  250V	8120-4211 8120-4600	Straight SABS164 90°	79/200 79/200	Jade Gray	Republic of South Africa India
OPT 918  100V	8120-4753 8120-4754	Straight Miti 90°	90/230 90/230	Dark Gray	Japan

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ART00019

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP part number for complete cable including plug.

**These cords are included in the CSA certification approval of the equipment.

E=Earth Ground
L=Line
N=Neutral

User Interface

The front-panel user interface of the HP 1652B/1653B consists of the front-panel keys, the KNOB, and the display. The interface allows you to configure the logic analyzer, each analyzer (machine) within the logic analyzer, and the oscilloscope in the logic analyzer. It also displays acquired data and measurement results.

Using the front-panel interface is a process of:

- selecting the desired menu with menu keys.
- placing the cursor on the desired field within the menu by rotating the KNOB.
- displaying the field options or current data by pressing the SELECT key.
- selecting the desired option by rotating the KNOB or entering new data by using the KNOB or the keypad.
- Starting and stopping data acquisition by using the RUN and STOP keys.

For additional information on the user interface refer to the *HP 1652B/1653B Front-Panel Operation Reference* manual.

HP-IB Interfacing

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of IEEE Standard 488-1978, "Standard Digital Interface for Programming Instrumentation." HP-IB is a carefully defined interface that simplifies the integration of various instruments and computers into systems. The interface makes it possible to transfer messages between two or more HP-IB compatible devices. HP-IB is a parallel bus of 16 active signal lines divided into three functional groups according to function.

Eight signal lines, called data lines, are in the first functional group. The data lines are used to transmit data in coded messages. These messages are used to program the instrument function, transfer measurement data, and coordinate instrument operation. Input and output of all messages, in bit parallel-byte serial form, are also transferred on the data lines. A 7-bit ASCII code normally represents each piece of data.

Data is transferred by means of an interlocking "Handshake" technique which permits data transfer (asynchronously) at the rate of the slowest active device used in that transfer. The data byte control lines coordinate the handshaking and form the second functional group.

The remaining five general interface management lines (third functional group) are used to manage the devices connected to the HP-IB. This includes activating all connected devices at once, clearing the interface, and other operations.

The connections to the HP-IB connector on the rear panel are shown in figure 2-3.

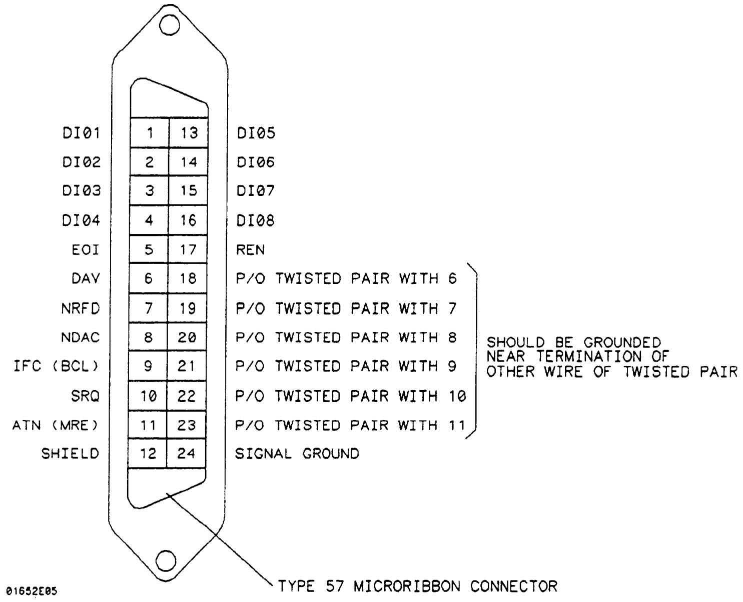
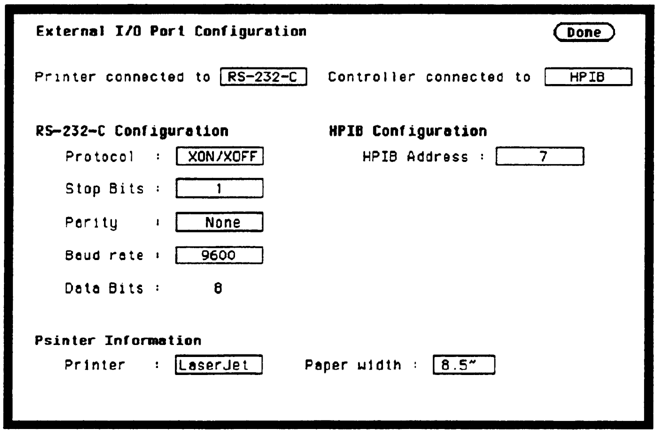

DI01
DI02
DI03
DI04
EOI
DAV
NRFD
NDAC
IFC (BCL)
SRQ
ATN (MRE)
SHIELD
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
DI05
DI06
DI07
DI08
REN
P/O TWISTED PAIR WITH 6
P/O TWISTED PAIR WITH 7
P/O TWISTED PAIR WITH 8
P/O TWISTED PAIR WITH 9
P/O TWISTED PAIR WITH 10
P/O TWISTED PAIR WITH 11
SIGNAL GROUND
SHOULD BE GROUNDED NEAR TERMINATION OF OTHER WIRE OF TWISTED PAIR
TYPE 57 MICRORIBBON CONNECTOR
01652E05

Figure 2-3. HP-IB Interface Connector

HP-IB Address Selection

Each instrument connected to the HP-IB interface bus requires a unique address. The address provides a method for the system controller to select individual instruments on the bus. The address of the HP 1652B/1653B defaults at power up to decimal "07." To change the address of the HP 1652B/1653B proceed as follows:

1. Press the I/O key on the front-panel keypad and the I/O menu will appear on screen.
2. Rotate the KNOB until "I/O Port Configuration" is highlighted.
3. Touch the SELECT key and the External I/O Port Configuration menu will appear on screen.



External I/O Port Configuration

Done

Printer connected to RS-232-C

Controller connected to HPIB

RS-232-C Configuration

Protocol : XON/XOFF

Stop Bits : 1

Parity : None

Baud rate : 9600

Data Bits : 8

HPIB Configuration

HPIB Address : 7

Printer Information

Printer : LaserJet

Paper width : 8.5"

Figure 2-4. External I/O Port Configuration Menu

4. Select the HP-IB Address field with the KNOB and press the SELECT key.
5. When the pop-up field appears on screen, rotate the KNOB to select the desired HP-IB address.

6. Touch the SELECT key to enter the new address.
7. Select the DONE field in the upper-right corner of the menu using the KNOB and SELECT key to exit the External I/O Port Configuration menu.

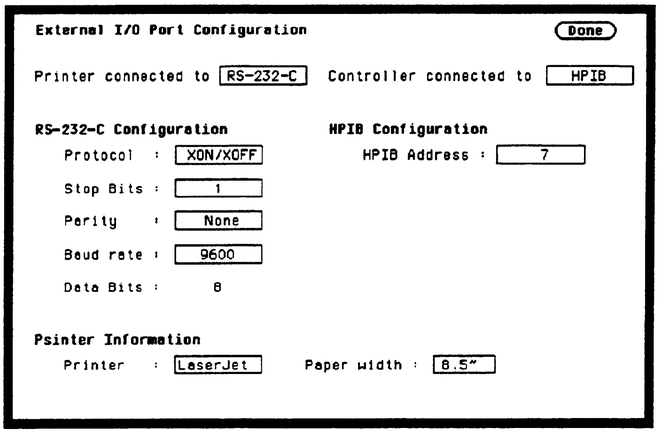
RS-232-C Interface

The HP 1652B/1653B interfaces with RS-232-C communication lines through a standard 25 pin D connector. The HP 1652B/1653B is compatible with RS-232-C protocol. When a hardwire handshake method is used, the Data Terminal Ready (DTR) line (pin 20 on the Computer/Modem connector) is used to signal whether space is available for more data in the logical I/O buffer. Pin outs of the RS-232-C connectors are listed in table 2-2.

RS-232-C Configuration

At power up, the RS-232-C interface is configured as shown in figure 2-5. To change the RS-232-C configuration:

1. Press the I/O key on the front-panel keypad and the I/O menu will appear on screen.
2. Rotate the KNOB until "I/O Port Configuration" is highlighted.
3. Touch the SELECT key and the External I/O Port Configuration menu will appear on screen.



Printer connected to RS-232-C
Controller connected to HPIB

RS-232-C Configuration
Protocol : XON/XOFF
Stop Bits : 1
Parity : None
Baud rate : 9600
Data Bits : 8

HPIB Configuration
HPIB Address : 7

Psinter Information
Printer : LaserJet
Paper width : 8.5"

Figure 2-5. External I/O Port Configuration Menu

4. Using the KNOB and SELECT key, configure the RS-232-C interface as desired.
5. Select the DONE field in the upper-right corner of the menu using the KNOB and SELECT key to exit the External I/O Port Configuration menu.

Table 2-2. RS-232-C Signal Definitions

Pin No.	Function	RS-232-C Standard	Signal Direction and Level
1	Protective Ground	AA	Not applicable
2	Transmitted Data (TD)	BA	Data from Mainframe High = Space = "0" = +12 V Low = Mark = "1" = -12 V
3	Received Data (RD)	BB	Data to Mainframe High = Space = "0" = +3 V to +25 V Low = Mark = "1" = -3 V to -25 V
4	Request to Send (RTS)	CA	Signal from Mainframe High = ON = +12 V Low = OFF = -12 V
5	Clear to Send (CTS)	CB	Signal to Mainframe High = ON = +3 V to +12 V Low = OFF = -3 V to -25 V
6	Data Set Ready (DSR)	CC	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = -3 V to -25 V
7	Signal Ground	AB	Not applicable
8	Data Carrier Detect (DCD)	CF	Signal to Mainframe High = ON = +3 V to +25 V Low = OFF = -3 V to -25 V
20	Data Terminal Ready (DTR)	CD	Signal from Mainframe High = ON = +12 V Low = OFF = -12 V
23	Data Signal Rate Selector	CH/CI	Signal from Mainframe Always High = ON = +12 V

Degaussing the Display

If the instrument has been subjected to strong magnetic fields, the CRT may become magnetized and display data may become distorted. To correct this condition, it may be necessary to degauss the CRT with a conventional external television type degaussing coil.

Operating Environment

The operating environment for the HP 1652B/1653B is described in section 1 of this manual. Note the non-condensing humidity limitation. Condensation within the instrument cabinet can cause poor operation or malfunction. Protection should be provided against temperature extremes which cause condensation within the instrument.

The HP 1652B/1653B will operate at all specifications within the temperature and humidity range given in section 1 of this manual.

Storage and Shipment

The instrument may be stored or shipped in environments within the following limits:

Temperature:	-40° C to +75° C.
Humidity:	Up to 90% at 65° C.
Altitude:	Up to 15,300 meters (50,000 feet).

Tagging for Service

If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag to the instrument identifying the owner, address of the owner, complete instrument model and serial numbers, and a description of the service required.

Original Packaging

If the original packaging material is unavailable or unserviceable, materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for service, attach a tag identifying the owner, address of the owner, complete instrument model and serial numbers, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

Other Packaging

The following general instructions should be followed for repacking the instrument with commercially available materials.

- Remove the disk from disk drive and install a yellow shipping disk.
- Wrap the instrument in heavy paper or plastic.
- Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.
- Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the control panel with cardboard.
- Seal the shipping container securely.
- Mark the shipping container FRAGILE to ensure careful handling.
- In any correspondence, refer to the instrument by model number and serial number.

Cleaning Requirements

Use MILD SOAP AND WATER to clean the HP 1652B/1653B cabinet and front panel. Care must be taken to not use a harsh soap which may damage the water-base paint finish of the instrument.

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3

Performance Tests

Introduction

The procedures in this section test the instrument's electrical performance by using the specifications listed in section 1 as the performance standards. All tests may be performed without access to the interior of the instrument.

Recommended Test Equipment

Equipment required for the performance tests in this section are listed in the Recommended Test Equipment table in section 1. Any equipment that satisfies the critical specification listed in the table may be substituted for the recommended model.

Test Record

The results of the performance tests may be tabulated on the Performance Test Record provided at the end of this section. The Performance Test Record lists the performance tests and provides an area to mark whether the test passed or failed. The results recorded in the table at incoming inspection may be used for later comparisons of the tests during periodic maintenance, troubleshooting, and after repairs or adjustments.

Self Tests

The power-up self test is automatically performed upon applying power to the logic analyzer. Self tests do not require test equipment and may be performed individually to provide a higher level of confidence that the instrument is operating properly. A message that the instrument has failed the test will appear if any problem is encountered during the test. The individual self tests may be performed for functions listed in the self test menu which is invoked via the I/O menu. Since the HP 1652B/1653B self test is located on the Performance Verification disk, you must have the Performance Verification disk installed to run the tests.

Power-up Self Test

The power-up self test is automatically invoked at power-up of the HP 1652B/1653B Logic Analyzer. The revision number of the operating system firmware is given in the upper right of the screen during the power-up self test. As each test is completed, either "passed" or "failed" will be printed in front of the name of the test in this manner:

```
PERFORMING POWER-UP SELF TESTS

  passed  ROM test
  passed  RAM test
  passed  Interrupt test
  passed  Display test
  passed  Keyboard test
  passed  Acquisition test
  passed  Threshold test
  passed  Disk test

LOADING SYSTEM FILE
```

As indicated by the last message, the HP 1652B/1653B will automatically load from the operating system disk in the disk drive. If the operating system disk is not in the disk drive, the message "SYSTEM DISK NOT FOUND" will be displayed at the bottom of the screen and "NO DISK" will be displayed in front of disk test in place of "passed".

If the message "SYSTEM DISK NOT FOUND" appears on screen, insert the operating system disk into the disk drive, and press any front-panel key.

Selectable Self Tests

Eight self tests may be invoked individually via the Self Test menu. The eight selectable self tests are:

- Analyzer Data Acquisition
- Scope Data Acquisition
- RS-232-C
- BNC
- Keyboard
- RAM
- ROM
- Disk Drive
- Cycle through tests

After entering the I/O Self Tests menu, the required test is selected by moving the cursor to the test and pressing the front panel SELECT key. A pop-up menu appears with a description of the test to be performed. The self test does not begin until the cursor is placed on Execute, Single test, or Repetitive test and the front panel SELECT key is pressed.

After the test has been completed, either "Passed", "Failed", or "Tested" will be displayed on the Self Test menu in front of the test. These self tests are used as troubleshooting aids. For more information, refer to section 6.

Performance Test Interval

Periodic performance verification of the HP 1652B/1653B is required at two year intervals. The instrument's performance should be verified after it has been serviced, or if improper operation is suspected. Calibration should be performed before any performance verification tests. Further checks requiring access to the interior of the instrument are included in the adjustment section, but are not required for the performance verification.

Performance Test Procedures

All performance tests should be performed at the instrument's environmental operating temperature and after a 15 minute warm up. The performance tests for the HP 1652B/1653B are separated into two sections. The first section contains the performance verification tests for the logic analyzer portion of the HP 1652B/1653B and the second section contains the performance verification tests for the oscilloscope portion. Procedures are based on the model or part number for the recommended equipment.

Logic Analyzer Performance Tests

These procedures test the electrical performance of the logic analyzer by using the specifications in section 1 as the performance standards. All tests may be performed without access to the interior of the instrument. Results of performance tests may be tabulated in the Performance Test Record at the end of this section.

Test Connector

The logic analyzer performance tests and adjustments require connecting the pulse generator outputs to probe pod inputs. Figure 3-1 is a test connector that may be built to allow testing of multiple channels (up to eight at one time). The test connector consists of a BNC connector and a length of wire. Connecting more than eight channels to the test connector at a time will induce loading of the circuit and true signal representation will degrade. Test results may not be accurate if more than eight channels are connected to the test connector.

The Hewlett-Packard part number for the BNC connector in figure 3-1 is 1250-1032. An equivalent part may be used in place of the Hewlett-Packard part.

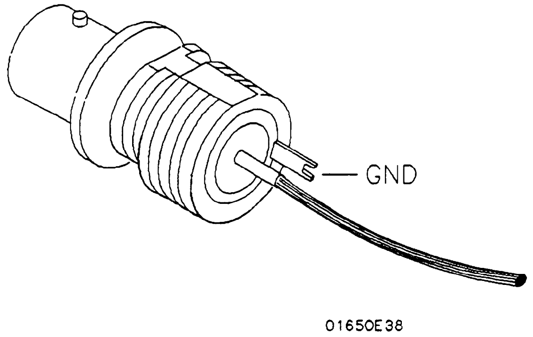


Figure 3-1. Test Connector

For quicker connection without the use of grabbers, a test connector may be built as shown in figure 3-2 to allow testing of multiple channels (up to eight at one time). The test connector consists of a BNC connector and a 2-by-8 Berg connector. The Hewlett-Packard part number for the BNC connector in figure 3-2 is 1250-1032 and the Hewlett-Packard part number for the 2-by-8 Berg connector is 1252-1816. Equivalent parts may be used in place of the Hewlett-Packard parts.

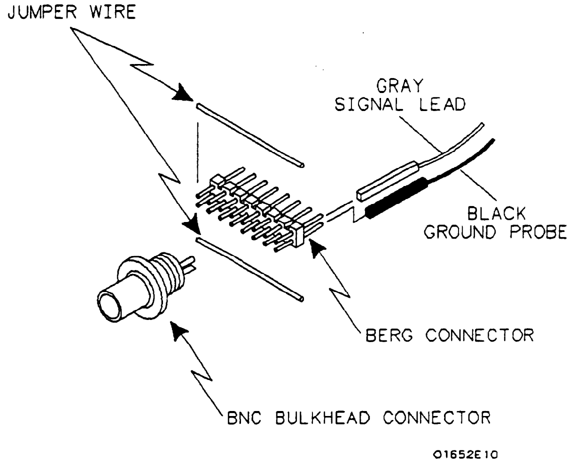


Figure 3-2. Test Connector Using Berg Connector

Clock, Qualifier, and Data Inputs Test 1

Description:

This test verifies the setup and hold times for the falling edge of the HP 1652B L clock specification, and the falling edge of the HP 1653B J and K clock specification. This test also verifies the maximum clock rate with counting mode on.

Specification:

Clock repetition rate: With time or state counting mode on, minimum time between states is 60 ns.

Setup time: Data must be present prior to the clock transition, ≥ 10 ns.

HP 1652B hold time: Data must be present after the falling edge of the L clock transition, 0 ns.

HP 1653B hold time: Data must be present after the falling edge of the J and K clock transition, 0 ns.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough (2)	HP 10100C
Test Connector (2)	see figure 3-1 and 3-2
BNC m-m Coupler (2)	HP 1250-0216
BNC Cable (2)	HP 10503A
BNC Tee m-f-f (2)	HP 1250-0781

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-3.

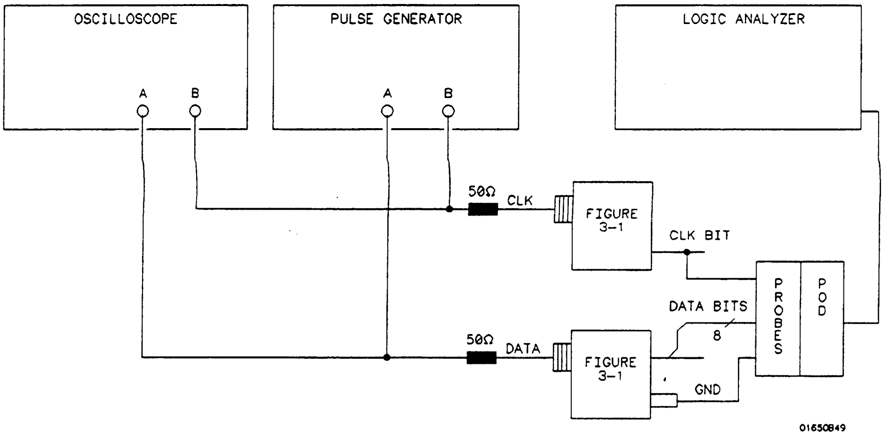

OSCILLOSCOPE
A
B
PULSE GENERATOR
A
B
LOGIC ANALYZER
50Ω
CLK
FIGURE 3-1
CLK BIT
DATA BITS
8
50Ω
DATA
FIGURE 3-1
GND
PROBES
POD
01650B49

Figure 3-3. Setup for Data Test 1

Note

In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be connected to ensure accurate test results.

---

2. Adjust the pulse generator for the output in figure 3-4.

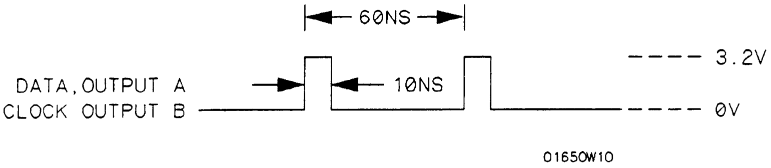
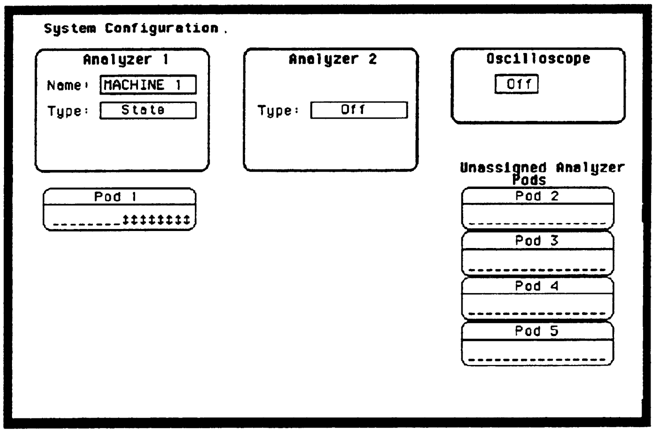

60NS
DATA, OUTPUT A
CLOCK OUTPUT B
10NS
3.2V
0V
01650W10

Figure 3-4. Waveform for Data Test 1

Setting for HP 8161A:

Parameter	**Output A**	**Output B**
Input Mode	Norm	---
Period (PER)	60 ns	---
Width (WID)	10 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	0 ns	0 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** menu as in figure 3-5. Refer to steps a through c if you are unfamiliar with menus.


System Configuration

Analyzer 1
Name: MACHINE 1
Type: State

Analyzer 2
Type: Off

Oscilloscope
Off

Pod 1
--------‡‡‡‡‡‡‡‡
Unassigned Analyzer Pods
Pod 2
Pod 3
Pod 4
Pod 5

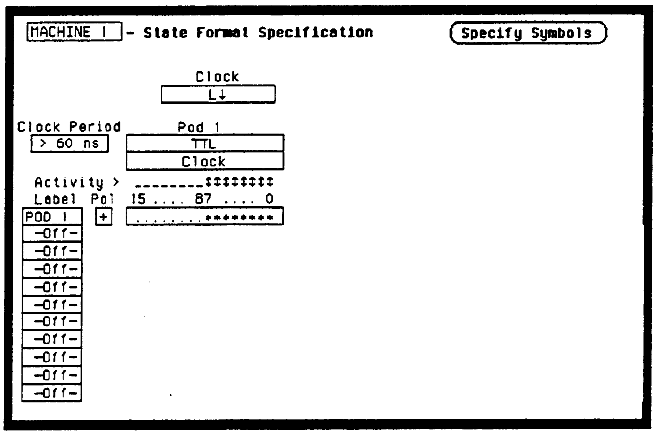
Figure 3-5. System Configuration for Data Test 1

a. Move the cursor to the **Type** field of **Analyzer 1** and press SELECT.

b. Set the analyzer **Type** to **State** using the cursor and the SELECT key.

c. Move the cursor to the **Pod** to be tested and assign it to **Machine 1.**

4. In the **State Format Specification** assign the **Clock Period** to **> 60 ns**. Also assign the lower 8 channels of the pod under test to a label as shown in figure 3-6. If you are testing the HP 1652B, assign the falling edge of the L clock for all pods. If you are testing the HP 1653B, assign the falling edge of the J clock for all pods. Refer to steps a through c if you are unfamiliar with the menus.



MACHINE 1 - State Format Specification

Specify Symbols

Clock L↓

Clock Period > 60 ns

Pod 1 TTL Clock

Activity > --------‡‡‡‡‡‡‡‡

Label Pol 15 .... 87 0

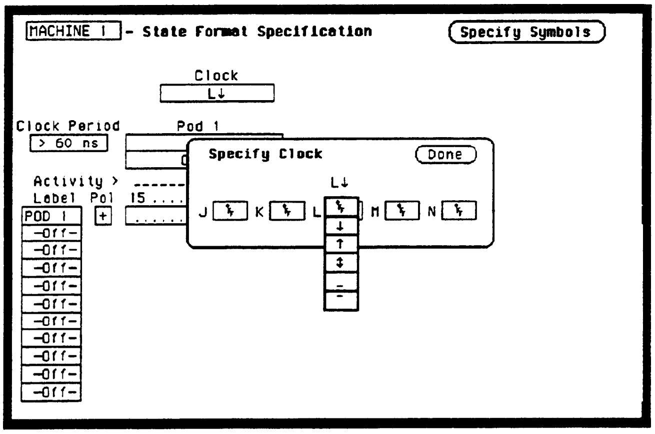
POD 1 + ...********

-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-

Figure 3-6. Format Specification for Data Test 1

a. Press the front-panel FORMAT/CHAN key.

b. Move the cursor to **Clock** field. Then use the cursor and SELECT key to assign the falling edge of the appropriate clock as in figure 3-7.



MACHINE 1 - State Format Specification

Specify Symbols

Clock L↓

Clock Period > 60 ns

Pod 1

Activity > ------

Label Pol 15 ....

POD 1 + ...

-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-

Specify Clock

Done

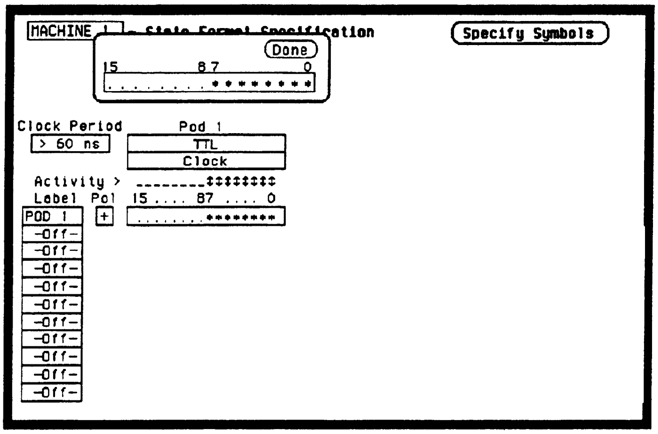
L↓

J ⍀ K ⍀ L ⍀ M ⍀ N ⍀

↓
↑
↕
-
‾

Figure 3-7. Clock Assignment for Data Test 1

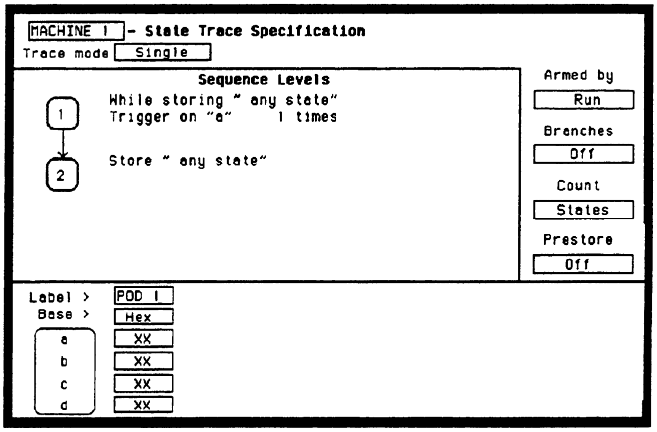
c. Move the cursor to the bit assignment field and turn on the appropriate eight bits to be tested (* = on; . = off) as in figure 3-8.



```
MACHINE 1 - State Format Specification                Specify Symbols
                                      Done
          15         8 7        0
          . . . . . . . . * * * * * * * *

Clock Period        Pod 1
 > 60 ns            TTL
                    Clock

  Activity >  --------‡‡‡‡‡‡‡‡
  Label  Pol  15 .... 87 .... 0
 POD 1    +   ........********
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
```

Figure 3-8. Bit Assignment for Data Test 1

5. Set up the **State Trace Specification** without sequencing levels and set **Count States** as in figure 3-9. Refer to steps a through c if you are unfamiliar with menus.



```
MACHINE 1 - State Trace Specification
Trace mode  Single
                     Sequence Levels                     Armed by
                                                           Run
  1      While storing " any state"
         Trigger on "a"      1 times                    Branches
                                                           Off
  2      Store " any state"
                                                          Count
                                                          States

                                                         Prestore
                                                           Off
 Label >   POD 1
  Base >   Hex
   a       XX
   b       XX
   c       XX
   d       XX
```

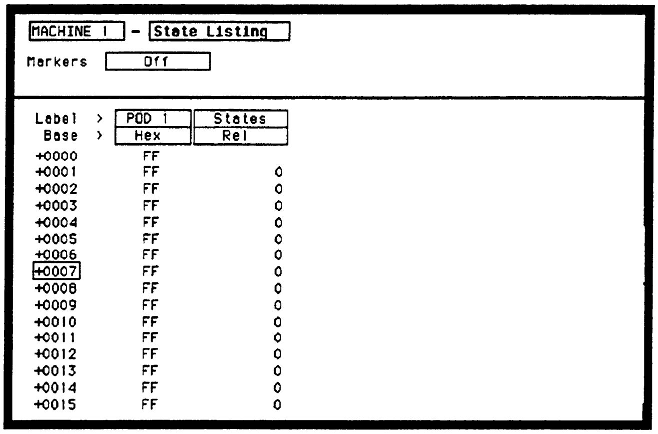
Figure 3-9. Trace Specification for Data Test 1

a. Press the front-panel TRACE/TRIG key.

b. Move the cursor to **Count** and press SELECT.

c. Move the cursor to **States**, press SELECT, and set it to **any state** by pressing SELECT again.

6. Press RUN. The **State Listing** is displayed and shows Fs for the channels under test as in figure 3-10.



```
MACHINE 1 - State Listing
Markers    Off

Label >  POD 1    States
 Base >   Hex      Rel
+0000     FF
+0001     FF         0
+0002     FF         0
+0003     FF         0
+0004     FF         0
+0005     FF         0
+0006     FF         0
+0007     FF         0
+0008     FF         0
+0009     FF         0
+0010     FF         0
+0011     FF         0
+0012     FF         0
+0013     FF         0
+0014     FF         0
+0015     FF         0
```

Figure 3-10. State Listing for Data Test 1

Note To ensure a consistent pattern of Fs in the listing, use the front-panel ROLL field and knob to scroll through the **State Listing**.

7. If you are testing the HP 1653B, connect the K clock of Pod 2 to the test connector and repeat steps 4 and 6 for the falling edge of the K clock.

8. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector. If you are testing the HP 1653B, reassign the falling edge of the J clock.

9. Repeat steps 3, 4, 6 and 7 until all of the pods have been tested.

10. Disconnect the lower eight bits (bits 0 through 7) from the test connector and attach the upper eight bits (bits 8 through 15) to the test connector.

11. Repeat steps 3, 4, 6, 7 and 8 until the upper bits of all pods have been tested.

Clock, Qualifier, and Data Inputs Test 2

Description:

This test verifies the setup and hold time specification for the rising edge transition of all of the clocks on the HP 1652B/1653B.

Specification:

Setup time: Data must be present prior to the clock transition, ≥ 10 ns.

Hold time: Data must be present after the rising clock transition, 0 ns.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough (2)	HP 10100C
Test Connector (2)	see figure 3-1 and 3-2
BNC m-m Coupler (2)	HP 1250-0216
BNC Cable (2)	HP 10503A
BNC Tee m-f-f (2)	HP 1250-0781

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-11.

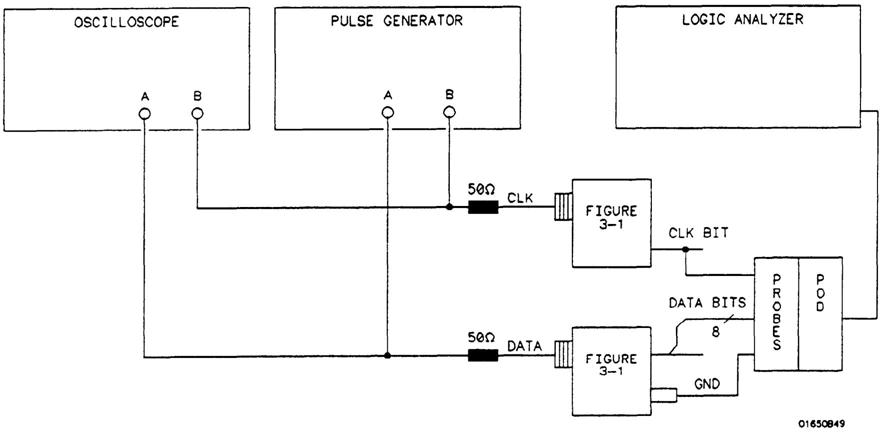

OSCILLOSCOPE
A
B
PULSE GENERATOR
A
B
LOGIC ANALYZER
50Ω
CLK
FIGURE 3-1
CLK BIT
PROBES
POD
DATA BITS
8
50Ω
DATA
FIGURE 3-1
GND
01650B49

Figure 3-11. Test Setup for Data Test 2

Note In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be connected to ensure accurate test results.

---

2. Adjust the pulse generator for the output in figure 3-12.

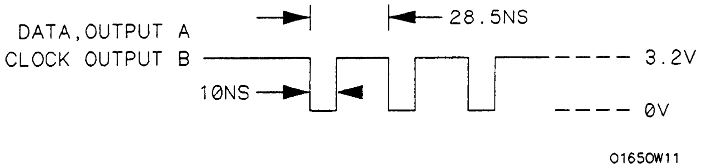


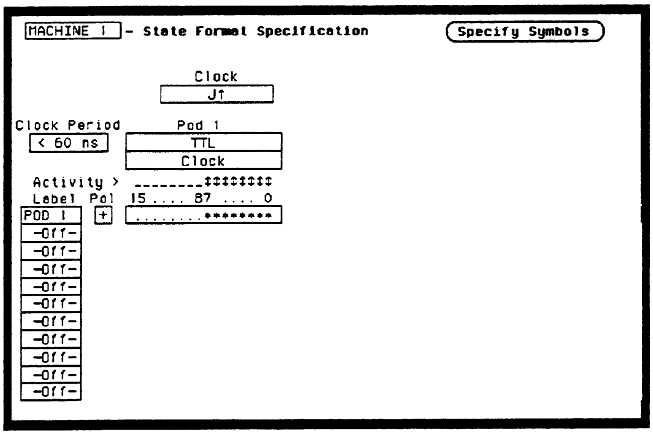
Figure 3-12. Waveform for Data Test 2

Setting for HP 8161A:

Parameter	**Output A**	**Output B**
Input Mode	Norm	---
Period (PER)		
HP 1652B	28.5 ns	---
HP 1653B	40.0 ns	---
Width (WID)	30 ns	30 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	0 ns	0 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in the previous test figure 3-5.

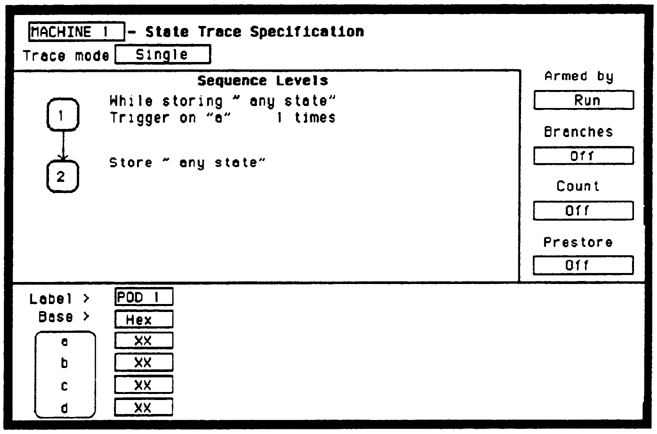
4. In the **State Format Specification** assign the **Clock Period** to **< 60 ns**, and assign the rising edge of the J clock to the **Clock** field. Also, assign the lower 8 channels of the pod under test to a label as in figure 3-13.



```
MACHINE 1 - State Format Specification              Specify Symbols

                    Clock
                     J↑

Clock Period        Pod 1
 < 60 ns             TTL
                    Clock

  Activity >  --------↕↕↕↕↕↕↕↕
  Label  Pol  15 .... 87 .... 0
POD 1     +   ........********
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
 -Off-
```

Figure 3-13. Format Specification for Data Test 2

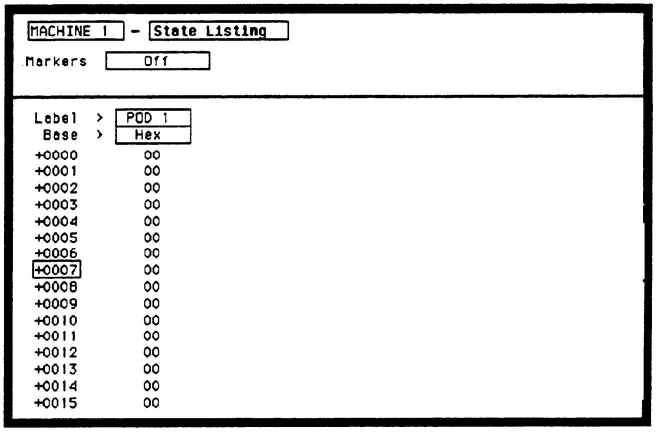
5. Set the **State Trace Specification** without sequencing levels and set **Count** to **Off** as in figure 3-14.



```
MACHINE 1 - State Trace Specification
Trace mode  Single
                    Sequence Levels                  Armed by
 1   While storing " any state"                        Run
     Trigger on "a"      1 times                     Branches
                                                       Off
 2   Store " any state"                              Count
                                                       Off
                                                     Prestore
                                                       Off
Label >  POD 1
Base  >  Hex
  a      XX
  b      XX
  c      XX
  d      XX
```

Figure 3-14. Trace Specification for Data Test 2

6. Press RUN. The **State Listing** is displayed and lists all 0s for the channels under test as in figure 3-15.



```
MACHINE 1 - State Listing
Markers    Off

Label  >  POD 1
Base   >  Hex
+0000      00
+0001      00
+0002      00
+0003      00
+0004      00
+0005      00
+0006      00
+0007      00
+0008      00
+0009      00
+0010      00
+0011      00
+0012      00
+0013      00
+0014      00
+0015      00
```

Figure 3-15. State Listing for Data Test 2

Note To ensure a consistent pattern of 0s in the listing, use the front-panel ROLL field and knob to scroll through the **State Listing**.

---

7. Connect the next clock to the test connector and repeat steps 4 and 6 for the appropriate clock. Repeat these steps until all clocks have been tested (clocks J, K, L, M and N).
8. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.
9. Repeat steps 3, 4, 6, and 7 until the lower bits of all pods (pods 1 through 5) have been tested with all clocks.
10. Disconnect the lower eight bits (bits 0 through 7) from the test connector. Attach the upper eight bits (bits 8 through 15) to the test connector and repeat steps 3, 4, 6, 7, and 8 until the upper bits of all pods (pods 1 through 5) have been tested with all clocks.

Clock, Qualifier, and Data Inputs Test 3 (HP 1652B Only)

Description:

This performance test verifies the hold time specification for the falling clock transitions of the J, K, M, and N clock on the HP 1652B.

Specification:

HP 1652B Hold time: Data must be present after the falling J, K, M, and N clock transition, 1 ns.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough (2)	HP 10100C
Test Connector (2)	see figure 3-1 and 3-2
BNC m-m Coupler (2)	HP 1250-0216
BNC Cable (2)	HP 10503A
BNC Tee m-f-f (2)	HP 1250-0781

Procedure:

1. Connect the HP 1652B and test equipment as in figure 3-16.

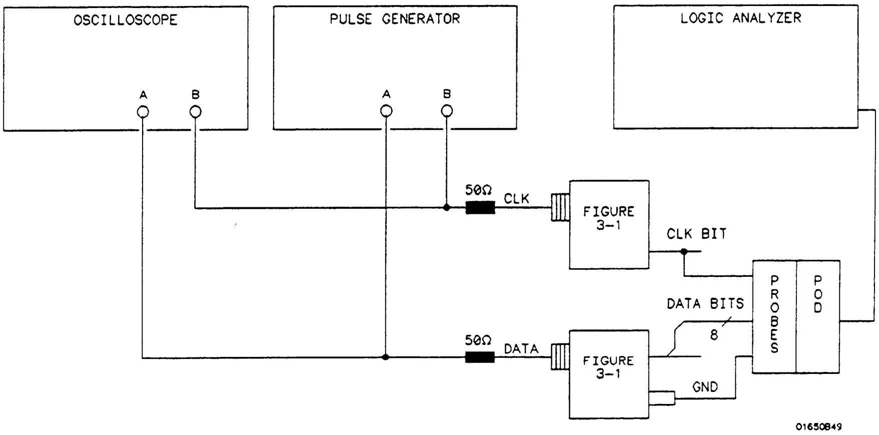

OSCILLOSCOPE
A
B
PULSE GENERATOR
A
B
LOGIC ANALYZER
50Ω
CLK
FIGURE 3-1
CLK BIT
PROBES
POD
DATA BITS
8
50Ω
DATA
FIGURE 3-1
GND
01650849

Figure 3-16. Setup for Data Test 3

Note

In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be connected to ensure accurate test results.

2. Adjust the pulse generator for the outputs in figure 3-17.

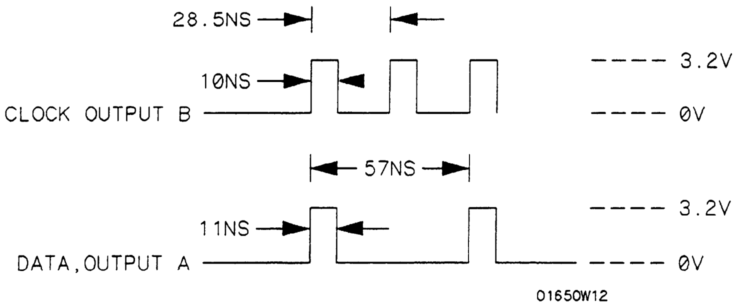


Figure 3-17. Waveform for Data Test 3

Setting for HP 8161A:

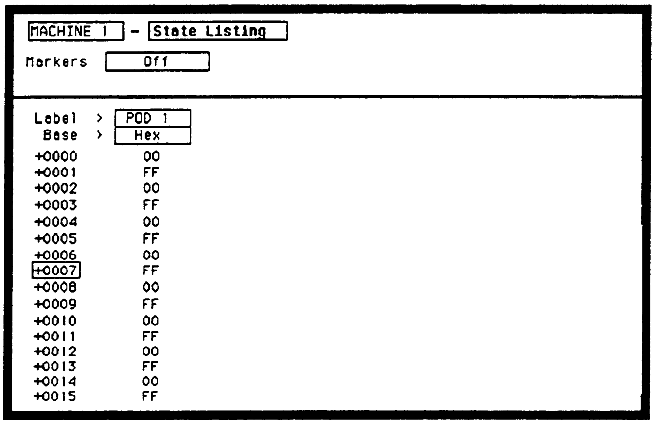
Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	57 ns	---
Width (WID)	11 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	0 ns	0 ns
Double Pulse (DBL)	---	28.5 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in the previous figure 3-5.

4. In the **State Format Specification** menu assign the **Clock Period** to **< 60 ns**, and the falling edge of J clock to the **Clock** field. Also, assign the lower 8 channels of the pod under test to a label as in the previous test figure 3-13.

5. Set the **State Trace Specification** without sequencing levels and set **Count** to **Off** as in the previous test figure 3-14.

6. Press RUN. The **State Listing** is displayed and lists alternating Fs and 0s as in figure 3-18.



```
MACHINE 1 - State Listing
Markers    Off

Label >  POD 1
 Base >   Hex
+0000     00
+0001     FF
+0002     00
+0003     FF
+0004     00
+0005     FF
+0006     00
+0007     FF
+0008     00
+0009     FF
+0010     00
+0011     FF
+0012     00
+0013     FF
+0014     00
+0015     FF
```

Figure 3-18. State Listing for Data Test 3

Note

To ensure a consistent pattern of alternating Fs and 0s, use the front-panel ROLL field and knob to scroll through the **State Listing**.

7. Connect the next clock to the test connector and repeat steps 4 and 6 for the appropriate clock. Repeat these steps until the J, K, M, and N clocks have been tested.
8. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector. Repeat steps 3, 4, 6, and 7 until all pods have been tested (pods 1 through 5).
9. Disconnect the lower eight bits (bits 0 through 7) from the test connector. Attach the upper eight bits (bits 8 through 15) to the test connector. Then repeat steps 3, 4, 6, 7, and 8 until the upper bits of all pods have been tested (pods 1 through 5).

Clock, Qualifier, and Data Inputs Test 4

Description:

This test verifies the minimum swing voltages of the input probes and the maximum clock rate of the HP 1652B/1653B when it is in the single phase mode.

Specification:

Minimum swing: 600 mV peak-to-peak.

Clock repetition rate: Single phase is 35 MHz maximum (25 MHz maximum for the HP 1653B).

Clock pulse width: ≥ 10 ns at threshold.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough (2)	HP 10100C
Test Connector (2)	see figure 3-1 and 3-2
BNC m-m Coupler (2)	HP 1250-0216
BNC Cable (2)	HP 10503A
BNC Tee m-f-f (2)	HP 1250-0781

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-19. In order to most accurately measure the amplitude of the test signals from the pulse generator, high impedance scope probes should be used to look at the signal levels at the output of the pulse generator.

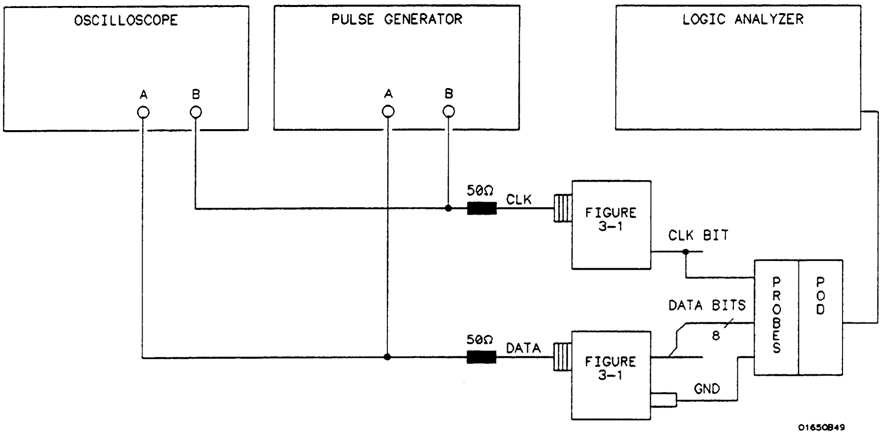

OSCILLOSCOPE
A
B
PULSE GENERATOR
A
B
LOGIC ANALYZER
50Ω
CLK
FIGURE 3-1
CLK BIT
PROBES
POD
DATA BITS
8
50Ω
DATA
FIGURE 3-1
GND
01650B49

Figure 3-19. Setup for Data Test 4

Note

In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be connected to ensure accurate test results. It is recommended that all eight channel grounds be connected.

---

2. Adjust the pulse generator for the output in figure 3-20.

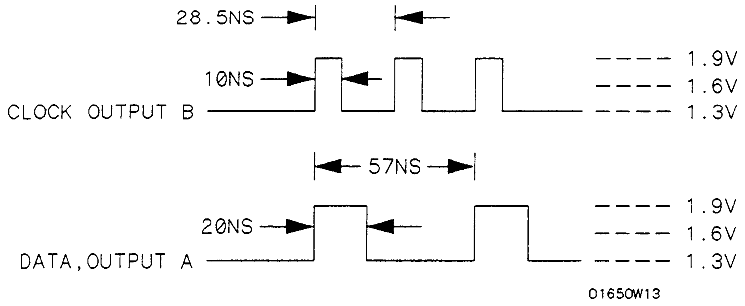


Figure 3-20. Waveform for Data Test 4

Setting for HP 8161A:

Parameter	**Output A**	**Output B**
Input Mode	Norm	---
Period (PER)		
HP 1652B	57 ns	---
HP 1653B	80 ns	---
Width (WID)	20 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	1.9V	1.9V (see Note)
Low Level (LOL)	1.3V	1.3V (see Note)
Delay (DEL)		
HP 1652B	18.5 ns	0 ns
HP 1653B	30 ns	0 ns
Double Pulse (DBL)		
HP 1652B	---	28.5 ns
HP 1653B	---	40 ns
Output Mode	ENABLE	ENABLE

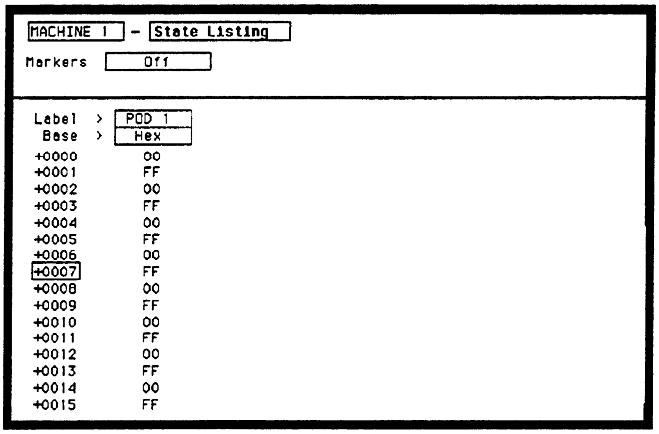
Note The voltage levels of the waveforms must have the correct amplitude at the logic analyzer probe tips. The pulse generator output may have to be increased slightly to compensate for loading by the logic analyzer.

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in the previous figure 3-5.

4. In the **State Format Specification** assign the **Clock Period** to **< 60 ns**, and the rising edge of the J clock to the **Clock** field. Also, assign the lower 8 channels of the pod under test to a label as in the previous figure 3-13.

5. Set the **State Trace Specification** without sequencing levels and set the **Count** to **Off** as in the previous figure 3-14.

6. Press RUN. The **State Listing** is displayed and shows alternating Fs and 0s for the channels under test as in figure 3-21.



```
MACHINE 1 - State Listing
Markers    Off

Label >  POD 1
 Base >   Hex
+0000     00
+0001     FF
+0002     00
+0003     FF
+0004     00
+0005     FF
+0006     00
+0007     FF
+0008     00
+0009     FF
+0010     00
+0011     FF
+0012     00
+0013     FF
+0014     00
+0015     FF
```

Figure 3-21. State Listing for Data Test 4

Note To ensure a consistent pattern of alternating Fs and 0s, use the front-panel ROLL field and knob to scroll through the **State Listing**.

---

7. Connect the next clock to the test connector and repeat steps 4 and 6 until all clocks have been tested (clocks J, K, L, M, and N).
8. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.
9. Repeat steps 3, 4, 6 and 7 until the lower bits of all pods have been tested (pods 1 through 5).
10. Disconnect the lower eight bits (bits 0 through 7) from the test connector and attach the upper eight bits (bits 8 through 15) to the test connector.
11. Repeat steps 3, 4, 6, 7, and 8 until the upper bits of all pods (pods 1 through 5) have been tested with all clocks.

Clock, Qualifier, and Data Inputs Test 5

Description:

This performance test verifies the maximum clock rate for mixed mode clocking during a state operation.

Specification:

Clock repetition rate: Single phase is 35 MHz maximum (25 MHz maximum for the HP 1653B). With time or state counting, minimum time between states is 60 ns (16.7 MHz maximum). Both mixed and demultiplexed clocking use master-slave clock timing. The master clock must follow the slave clock by at least 10 ns and precede the next slave clock by 50 ns.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough (2)	HP 10100C
Test Connector (2)	see figure 3-1 and 3-2
BNC m-m Coupler (2)	HP 1250-0216
BNC Cable (2)	HP 10503A
BNC Tee m-f-f (2)	HP 1250-0781

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-22 by connecting channels 0-3 and 8-11 of the pod under test to the test connector. On the slave clock transition, the four bits of the lower byte are transferred to the logic analyzer. On the master clock transition, the four bits of the upper byte are transferred to the logic analyzer.

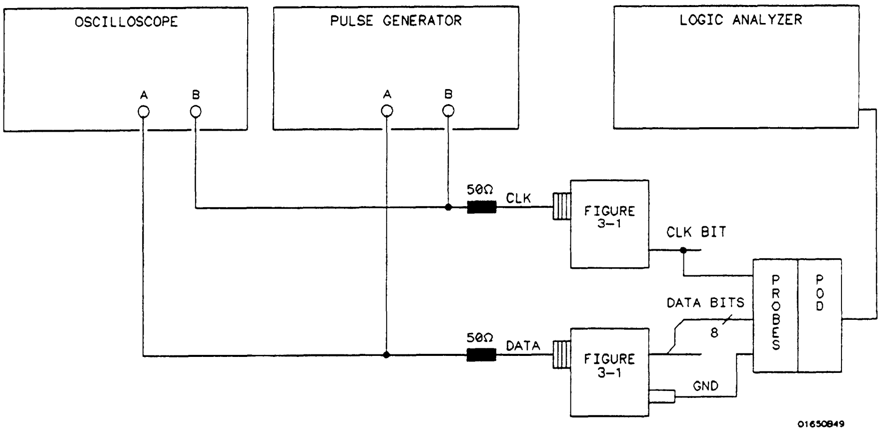


Figure 3-22. Setup for Data Test 5

Note

In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be connected to ensure accurate test results.

2. Adjust the pulse generator for the output in figure 3-23.

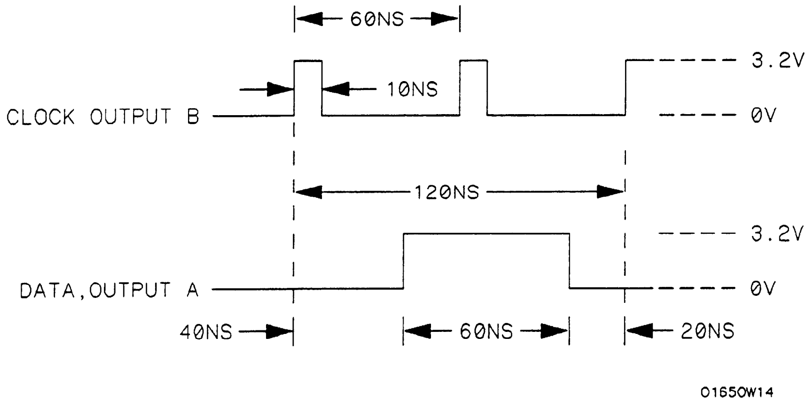

60NS
3.2V
10NS
CLOCK OUTPUT B
0V
120NS
3.2V
DATA,OUTPUT A
0V
40NS
60NS
20NS
01650W14

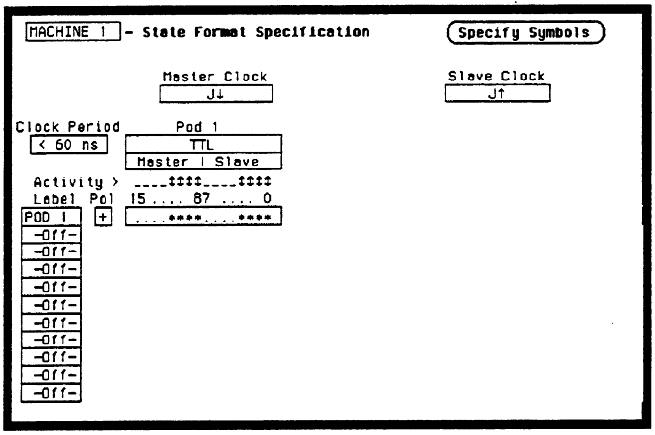
Figure 3-23. Waveform for Data Test 5

Setting for HP 8161A:

Parameter	Output A	Output B
Input Mode	Norm	---
Period (PER)	120 ns	---
Width (WID)	60 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	40 ns	0 ns
Double Pulse (DBL)	---	60 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in the previous figure 3-5.

4. Set up the **State Format Specification** as in figure 3-24. Assign the falling J clock to the **Master Clock** and the rising J clock to the **Slave Clock**. Refer to steps a through d after figure 3-24 if you are unfamiliar with menus.



MACHINE 1 - State Format Specification

Master Clock: J↓

Slave Clock: J↑

Clock Period: < 60 ns

Pod 1: TTL, Master | Slave

Activity > ____‡‡‡‡____‡‡‡‡

Label Pol 15 .... 87 0

POD 1 + ...****....****

Specify Symbols
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-

Figure 3-24. Format Specification for Data Test 5

   a. Move the cursor to the **Pod Clock** field and press SELECT. Then assign **Mixed Clocks**.

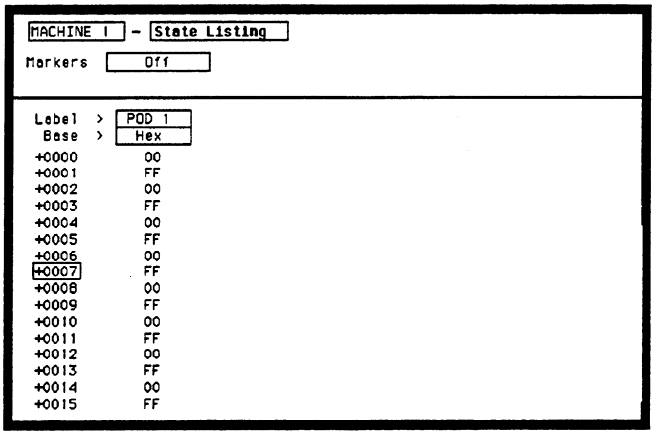
   b. Move the cursor to the clock fields and assign the falling transition of the J clock to the **Master Clock** and the rising transition of the J clock to the **Slave Clock**.

   c. Move the cursor to the appropriate bit assignment field and turn on channels 0-3 and 8-11 of the pod under test.

   d. Move the cursor to the **Clock Period** and set it to **< 60 ns**.

5. Set the **State Trace Specification** without sequencing levels and **Count Off** as in the previous figure 3-14.

6. Press RUN. The **State Listing** displays alternating Fs and 0s for the channels under test as in figure 3-25.



```
MACHINE 1 - State Listing
Markers    Off

 Label  >  POD 1
  Base  >   Hex
+0000        00
+0001        FF
+0002        00
+0003        FF
+0004        00
+0005        FF
+0006        00
+0007        FF
+0008        00
+0009        FF
+0010        00
+0011        FF
+0012        00
+0013        FF
+0014        00
+0015        FF
```

Figure 3-25. State Listing for Data Test 5

Note To ensure a consistent pattern of alternating Fs and 0s, use the front-panel ROLL field and knob to scroll through the **State Listing**.

---

7. Connect the next clock to the test connector and repeat steps 4 and 6. Repeat these steps until all clocks have been tested (clocks J, K, L, M, and N).

8. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.

9. Repeat steps 3, 4, 6, and 7 until channels 0 - 3 and 8 - 11 of all pods have been tested (pods 1 through 5). Start with the falling edge of the J clock as the Master clock and rising edge of the J clock as the Slave clock.

10. Disconnect bits 0-3 and bits 8-11 from the test connector and attach bits 4-7 and bits 12-15 to the test connector. Repeat steps 3, 4, 6, 7, and 8 until all pods have been tested (pods 1 through 5) with all clocks.

Clock, Qualifier, and Data Inputs Test 6

Description:

This performance test verifies the maximum clock rate for demultiplexed clocking during a state operation.

Specification:

Clock repetition rate: Single phase 35 MHz maximum (25 MHz maximum for the HP 1653B). With time or state counting, minimum time between states is 60 ns (16.7 MHz maximum). Both mixed and demultiplexed clocking use master-slave clock timing; the master clock must follow the slave clock by at least 10 ns and precede the next slave clock by 50 ns.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough (2)	HP 10100C
Test Connector (2)	see figure 3-1 and 3-2
BNC m-m Coupler (2)	HP 1250-0216
BNC Cable (2)	HP 10503A
BNC Tee m-f-f (2)	HP 1250-0781

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-26 by connecting channels 0-7 of the pod under test to the test connector. During demultiplexed clocking only the lower eight bits of each pod are used.

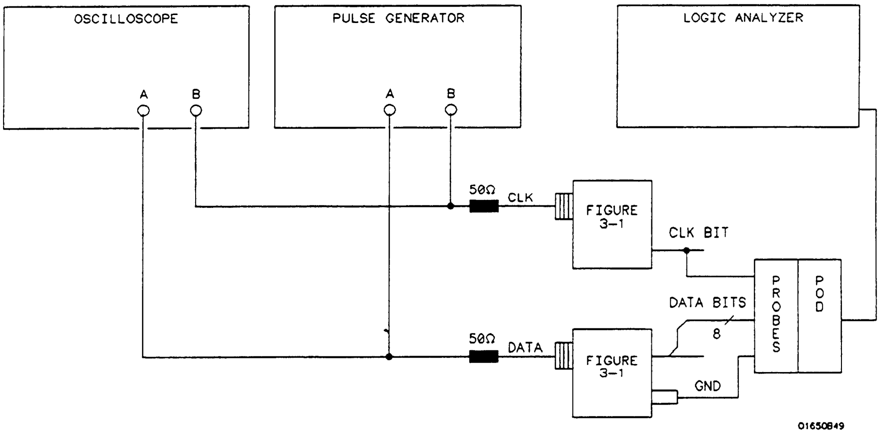
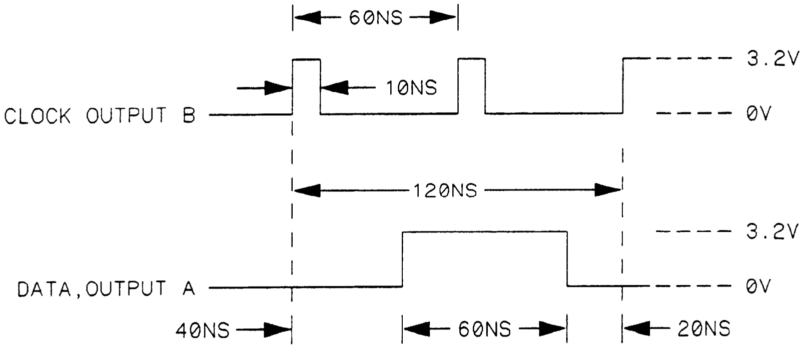

OSCILLOSCOPE
A
B
PULSE GENERATOR
A
B
LOGIC ANALYZER
50Ω
CLK
FIGURE 3-1
CLK BIT
DATA BITS
8
PROBES
POD
50Ω
DATA
FIGURE 3-1
GND
01650849

Figure 3-26. Setup for Data Test 6

2. Adjust the pulse generator for the output in figure 3-27.



01650W14

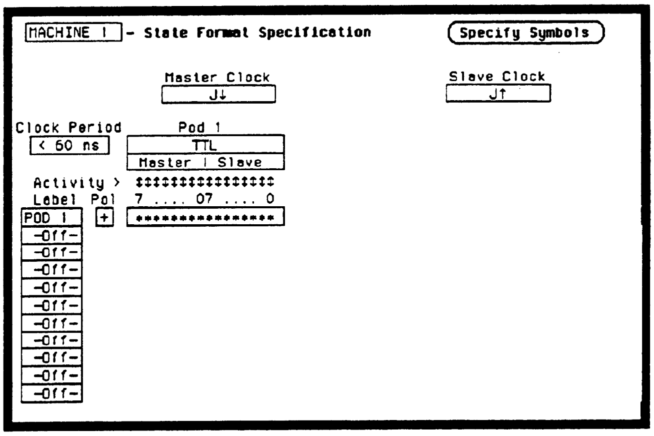
Figure 3-27. Waveform for Data Test 6

Setting for HP 8161A:

Parameter	**Output A**	**Output B**
Input Mode	Norm	---
Period (PER)	120 ns	---
Width (WID)	60 ns	10 ns
Leading Edge (LEE)	1 ns	1 ns
Trailing Edge (TRE)	1 ns	1 ns
High Level (HIL)	3.2 V	3.2 V
Low Level (LOL)	0 V	0 V
Delay (DEL)	40 ns	ns
Double Pulse (DBL)	---	60 ns
Output Mode	ENABLE	ENABLE

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in the previous figure 3-5.

4. Set up the **State Format Specification** as in figure 3-28. Assign the falling J clock as the **Master Clock** and the rising J clock as the **Slave Clock.** Refer to steps a through d if you are unfamiliar with the menus.


MACHINE 1 - State Format Specification
Specify Symbols

Master Clock: J↓
Slave Clock: J↑

Clock Period: < 60 ns
Pod 1: TTL
Master | Slave

Activity > ↕↕↕↕↕↕↕↕↕↕↕↕↕↕↕↕
Label Pol 7 .... 07 0
POD 1 + ****************
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-

Figure 3-28. Format Specification for Data Test 6

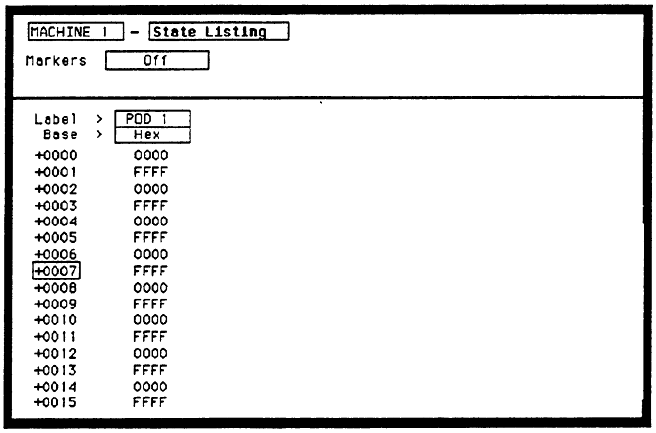
a. Move the cursor to the **Pod Clock** field, press SELECT, and assign **Demultiplex.**

b. Move the cursor to the clock fields and assign the falling clock transition of the J clock to the **Master Clock** and the rising J clock transition to the **Slave Clock.**

c. Move the cursor to the appropriate bit field and assign ALL channels to the pod under test (only bits 0 through 7 are available for assignment).

d. Move the cursor to the **Clock Period** and set it to **< 60 ns**.

5. Set the **State Trace Specification** without sequencing levels and set **Count Off** as in the previous figure 3-14.
6. Press RUN. The **State Listing** shows alternating Fs and 0s for the pod under test as in figure 3-29.



```
MACHINE 1 - State Listing
Markers    Off

Label >  POD 1
 Base >  Hex
+0000    0000
+0001    FFFF
+0002    0000
+0003    FFFF
+0004    0000
+0005    FFFF
+0006    0000
+0007    FFFF
+0008    0000
+0009    FFFF
+0010    0000
+0011    FFFF
+0012    0000
+0013    FFFF
+0014    0000
+0015    FFFF
```

Figure 3-29. State Listing for Data Test 6

Note To ensure a consistent pattern of alternating Fs and 0s, use the front-panel ROLL field and knob to scroll through the **State Listing.**

---

7. Connect the next clock to the test connector and repeat steps 4 and 6.
8. Repeat steps 4, 6, and 7 until all clocks have been tested (clocks J, K, L, M and N).
9. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.
10. Repeat steps 3, 4, 6, 7, 8, and 9 until all pods have been tested (pods 1 through 5). Start with the falling edge of the J clock as the **Master Clock** and rising edge of the J clock as the **Slave Clock.**

Glitch Test

Description:

This performance test verifies the glitch detection specification of the HP 1652B/1653B.

Specification:

Minimum detectable glitch: 5 ns wide at the threshold.

Equipment Required:

Pulse Generator	HP 8161A/020
Oscilloscope	HP 54502A
50 Ohm Feedthrough	HP 10100C
Test Connector	see figure 3-1 and 3-2
BNC m-m Coupler	HP 1250-0216
BNC Cable	HP 10503A
BNC Tee m-f-f	HP 1250-0781

Procedure:

1. Connect the test equipment as in figure 3-30. The clock inputs are not used for the glitch test since glitch detection is part of timing analysis. Use the oscilloscope to make sure pulses are 5 ns wide at the threshold (1.6 V).

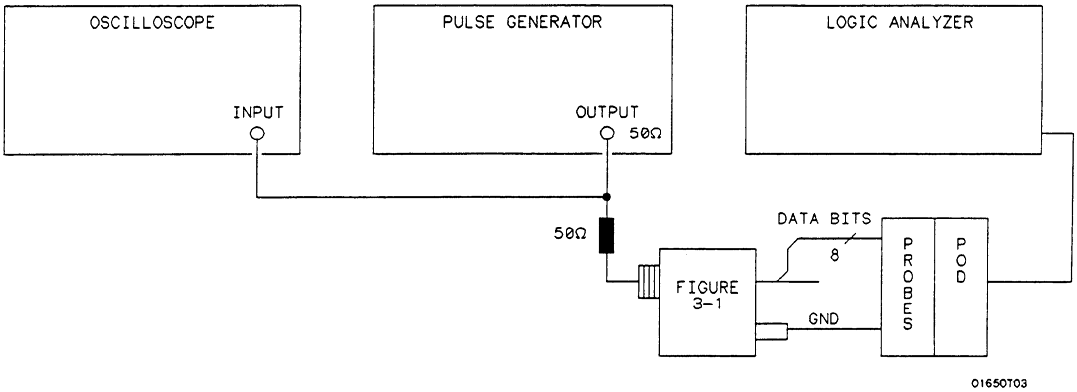
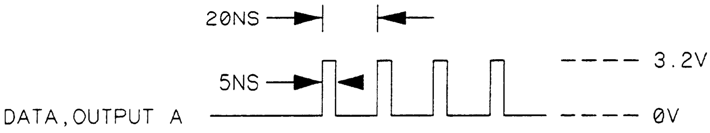

OSCILLOSCOPE
INPUT
PULSE GENERATOR
OUTPUT
50Ω
LOGIC ANALYZER
50Ω
FIGURE 3-1
DATA BITS
8
GND
PROBES
POD
01650T03

Figure 3-30. Setup for Glitch Test

Note

In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be connected to ensure accurate test results.

2. Adjust the pulse generator for the output in figure 3-31.


20NS
5NS
3.2V
DATA, OUTPUT A
0V

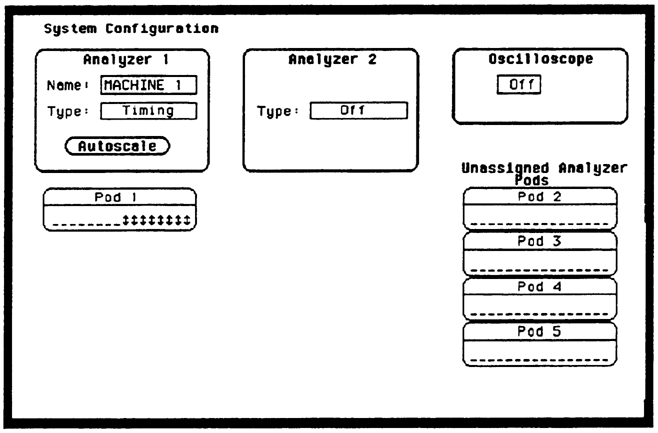
01650W15

Figure 3-31. Waveform for Glitch Test

Setting for HP 8161A:

Parameter	**Output A**	**Output B**
Input Mode	Norm	---
Period (PER)	20 ns	---
Width (WID)	5 ns	---
Leading Edge (LEE)	1 ns	---
Trailing Edge (TRE)	1 ns	---
High Level (HIL)	3.2 V	---
Low Level (LOL)	0 V	---
Delay (DEL)	0 ns	---
Output Mode	ENABLE	---

3. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in figure 3-32. Refer to steps a through c if you are unfamiliar with menus.



System Configuration

Analyzer 1
Name: MACHINE 1
Type: Timing

Analyzer 2
Type: Off

Oscilloscope
Off

Autoscale
Pod 1
--------‡‡‡‡‡‡‡‡
Unassigned Analyzer Pods
Pod 2
Pod 3
Pod 4
Pod 5

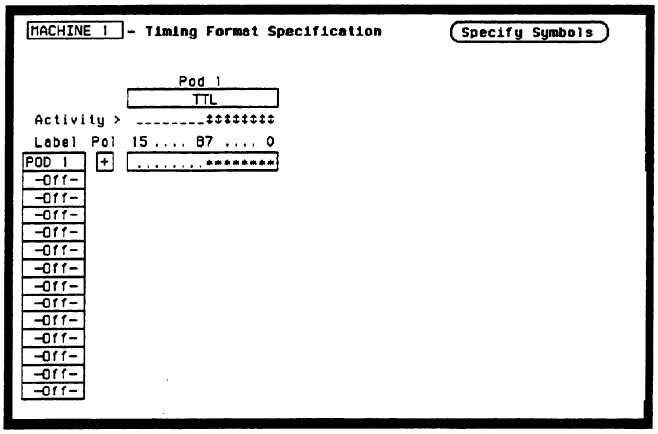
Figure 3-32. System Configuration for Glitch Test

a. Move the cursor to the **Type** field of **Analyzer 1** and press SELECT.

b. Set the analyzer **Type** to **Timing** using the cursor and SELECT key.

c. Move the cursor to the pod to be tested and assign it to **Machine 1** (Analyzer 1).

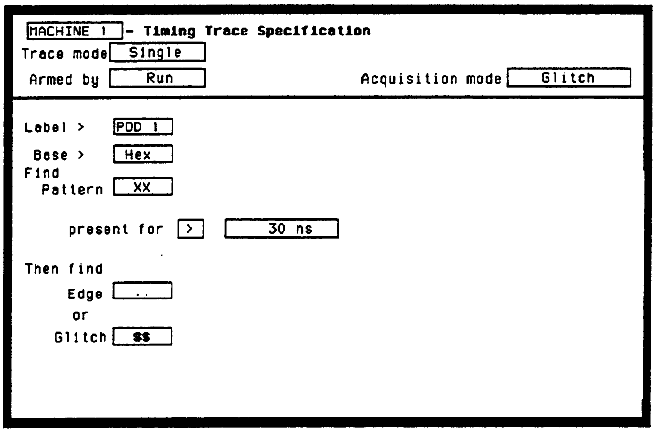
4. In **State Format Specification** assign the lower eight bits of the pod under test to a label as shown in figure 3-33. Make sure the appropriate eight bits in the bit assignment field are turned on.



```
MACHINE 1 - Timing Format Specification                Specify Symbols

                    Pod 1
                     TTL
Activity >   --------‡‡‡‡‡‡‡‡
Label  Pol   15 .... 87 .... 0
POD 1   +    ........********
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
```

Figure 3-33. Glitch Test Timing Format Specification

5. Set **Timing Trace Specification** as in figure 3-34. Follow steps a through d if you are unfamiliar with menus.



```
MACHINE 1 - Timing Trace Specification
Trace mode  Single
 Armed by    Run                       Acquisition mode   Glitch

Label >    POD 1

 Base >    Hex
Find
  Pattern  XX

     present for  >     30 ns

Then find
     Edge   ..
      or
   Glitch  $$
```

Figure 3-34. Glitch Test Timing Trace Specification

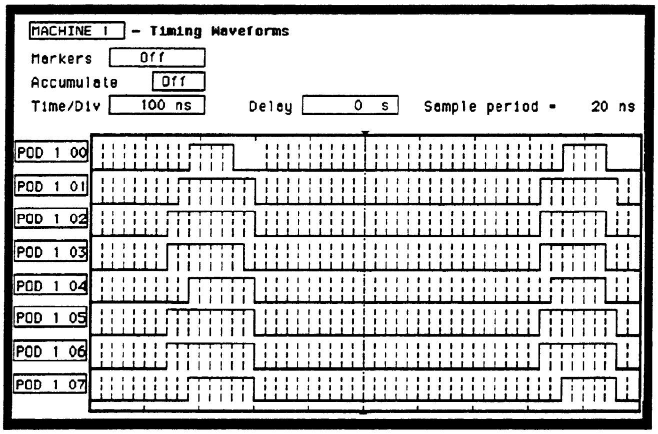
a. Move the cursor to the **Acquisition mode** field and select the **Glitch** mode.

b. Move the cursor to the **Find Pattern** field and press SELECT. Assign all Don't Cares (all Xs) and press SELECT.

c. Set the **Present for** field to **>30 ns.**

d. Set **Then find Glitch** "on" for all channels (* = on; . = off).

6. Press RUN. The timing analyzer acquires data and shows glitches for channels under test as in figure 3-35. Select the **Delay** field and rotate the knob to assure consistent glitch detection.


MACHINE 1 - Timing Waveforms

Markers Off

Accumulate Off

Time/Div 100 ns

Delay 0 s

Sample period = 20 ns

Figure 3-35. Glitch Test Timing Waveforms

Note

If the sample clock and data synchronize, glitches may be displayed on the timing screen as valid data transitions.

---

7. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.

8. Repeat steps 3, 4, and 6 until all pods have been tested (pods 1 through 5). Make sure to assign the correct pod to be tested in the **System Configuration** menu.

9. Disconnect the lower eight bits (bits 0 through 7) from the test connector and attach the upper eight bits (bits 8 through 15) to the test connector.

10. Repeat steps 3, 4, 6, and 7 until the upper bits of all pods have been tested (pods 1 through 5).

Threshold Accuracy Test

Description:

This performance test verifies the threshold accuracy within the ranges stated in the specification.

Specification:

Threshold accuracy: 150 mV accuracy over the range -2.0 to +2.0 volts; 300 mV accuracy over the ranges -9.9 to -2.1 volts and +2.1 to +9.9 volts.

Equipment Required:

Power Supply	HP 6216C
Test Connector	see figure 3-1 and 3-2
BNC (f)-to-Dual Banana (m) Adapter	HP 1251-2277
BNC Cable	HP 10503A

Procedure:

1. Connect the test equipment as in figure 3-36.

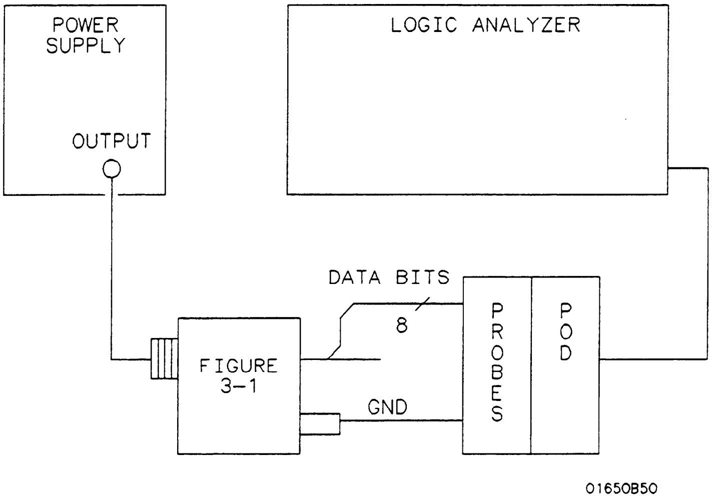


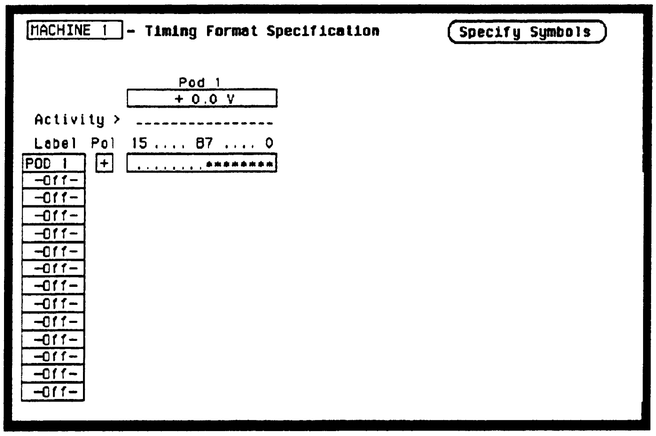
Figure 3-36. Threshold Accuracy Test Setup

Note In this setup, only eight channels are tested at one time to minimize loading. The ground lead must be grounded to ensure accurate test results.

---

2. Assign the pod under test to **Analyzer 1** in the **System Configuration** as in the previous figure 3-32.

3. Configure the **Timing Format Specification** for a **User Defined** pod threshold of **0.0 V** for the pod under test and assign the lower eight bits in the bit assignment field as in figure 3-37. Refer to steps a through c if you are unfamiliar with menus.



```
MACHINE 1 - Timing Format Specification          Specify Symbols

                 Pod 1
               + 0.0 V
Activity >   ----------------
Label  Pol   15 .... 87 .... 0
POD 1   +    ........********
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
-Off-
```

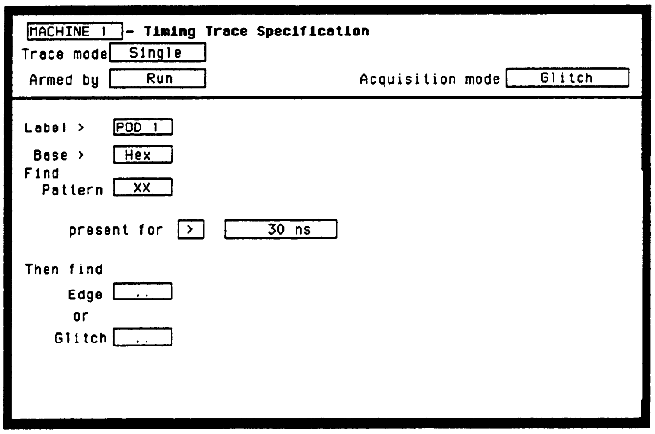
Figure 3-37. Threshold Accuracy Format Specification

a. Move the cursor to the Pod Threshold field and press SELECT.

b. Move the cursor to **User-defined** and press SELECT. Then enter the appropriate voltage threshold.

c. Move the cursor to the bit assignment field and turn on the appropriate eight bits to be tested (* = on; . = off).

4. Set the **Timing Trace Specification** as in figure 3-38. Follow steps a through d if you are unfamiliar with menus.



```
MACHINE 1 - Timing Trace Specification
Trace mode  Single
 Armed by    Run                    Acquisition mode   Glitch

Label >    POD 1
 Base >    Hex
Find
  Pattern  XX

     present for  >    30 ns

Then find
     Edge   ..
      or
   Glitch   ..
```

Figure 3-38. Threshold Accuracy Trace Specification

a. Move the cursor to the **Acquisition mode** and select the **Glitch** mode.

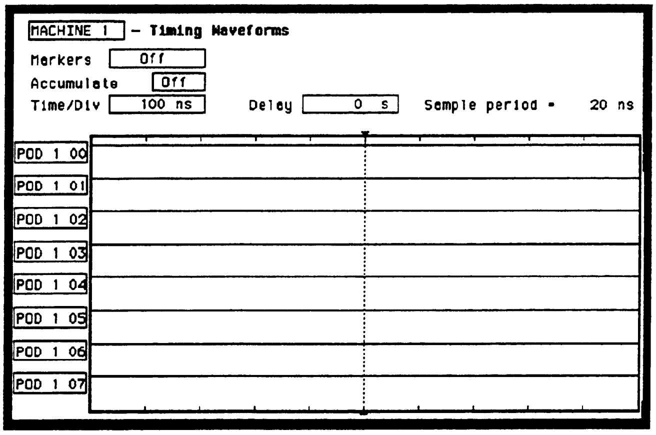
b. Move the cursor to **Find Pattern** and press SELECT. Then assign Don't Cares (all X s) and press SELECT.

c. Set **present for** to **>30 ns**.

d. Set **Then find Glitch** to all Don't Cares (all periods ".").

5. Adjust the power supply output for +150 mV.

6. Press RUN. Data displayed on the **Timing Waveforms** display is all high for the pod and channels under test as in figure 3-39.



MACHINE 1 - Timing Waveforms

Markers Off

Accumulate Off

Time/Div 100 ns

Delay 0 s

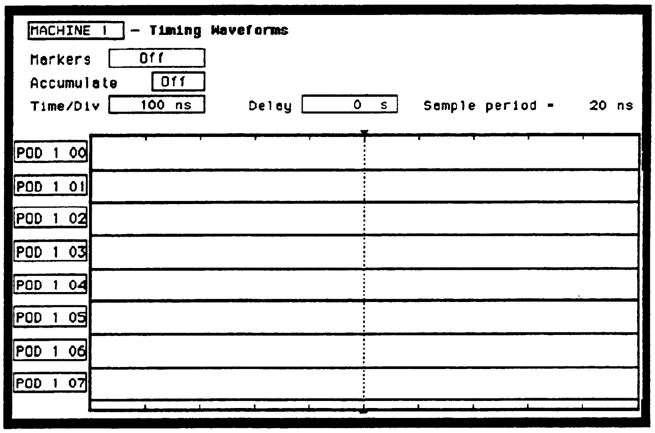
Sample period = 20 ns

POD 1 00
POD 1 01
POD 1 02
POD 1 03
POD 1 04
POD 1 05
POD 1 06
POD 1 07

Figure 3-39. Threshold Accuracy Timing Waveforms 1

7. Adjust the power supply output for -150 mV.

8. Press RUN. Data displayed on the **Timing Waveforms** display is all low for the channels under test as in figure 3-40.



MACHINE 1 - Timing Waveforms

Markers Off

Accumulate Off

Time/Div 100 ns

Delay 0 s

Sample period = 20 ns

POD 1 00
POD 1 01
POD 1 02
POD 1 03
POD 1 04
POD 1 05
POD 1 06
POD 1 07

Figure 3-40. Threshold Accuracy Timing Waveforms 2

9. Return to the **Timing Format Specification** and change the **User Defined** pod threshold to **+9.9** V.

10. Adjust the power supply output for +10.2 V.

11. Press RUN. Data displayed on **Timing Waveforms** display is all high for the pod and channels under test as in the previous figure 3-39.

12. Adjust the power supply output for +9.6 V.
13. Press RUN. Data displayed on **Timing Waveforms** display is all low for the pod and channels under test as in the previous figure 3-40.
14. Return to the **Timing Format Specification** and change the **User Defined** pod threshold to **-9.9** V.
15. Adjust the power supply output for -9.6 V.
16. Press RUN. Data displayed on **Timing Waveforms** display is all high for the pod and channels under test as in the previous figure 3-39.
17. Adjust the power supply output for -10.2 V.
18. Press RUN. Data displayed on **Timing Waveforms** display is all low for the pod and channels under test as in the previous figure 3-40.
19. Remove the probe tip assembly from the logic analyzer probe cable and attach it to the next logic analyzer probe cable to be tested. Take care not to dislodge grabbers from the test connector.
20. Repeat steps 2 through 18 until all pods have been tested (pods 1 through 5).
21. Disconnect the lower eight bits (bits 0 through 7) from test connector and attach the upper eight bits (bits 8 through 15) to the test connector.
22. Repeat steps 2 through 19 until the upper bits of all pods have been tested (pods 1 through 5).

Oscilloscope Performance Tests

These procedures test the HP 1652B/1653B oscilloscope module's electrical performance using the specifications listed in section 1 as the performance standards. All tests can be performed without access to the interior of the instrument. Results of performance tests may be tabulated in the Performance Test Record at the end of this section.

Input Resistance Test

Description:

This test checks the input resistance of the vertical inputs. A four-wire measurement is used for accuracy at 50 Ω. Input resistance is not a specification, but this test is provided for the convenience of the user.

Note

The Input Resistance Test is optional. The input resistance is not specified in the instrument performance specifications. The values given are typical. Results are not recorded in the test record.

Characteristic:

1 MΩ ±1% and 50 Ω ±1%

Equipment Required:

Digital Multimeter	HP 3478A
BNC Cable (2)	HP 10503A
BNC Tee m-f-f	HP 1250-0781
BNC (f)-to-Banana (m) Adapter (2)	HP 1251-2277

Procedure:

1. Set up the multimeter to make a four-wire resistance measurement.
2. Use the BNC-to-banana adapters to connect one end of each BNC cable to the four-wire resistance connections on the multimeter. Then connect the free ends of the cables to the BNC tee as in figure 3-41.

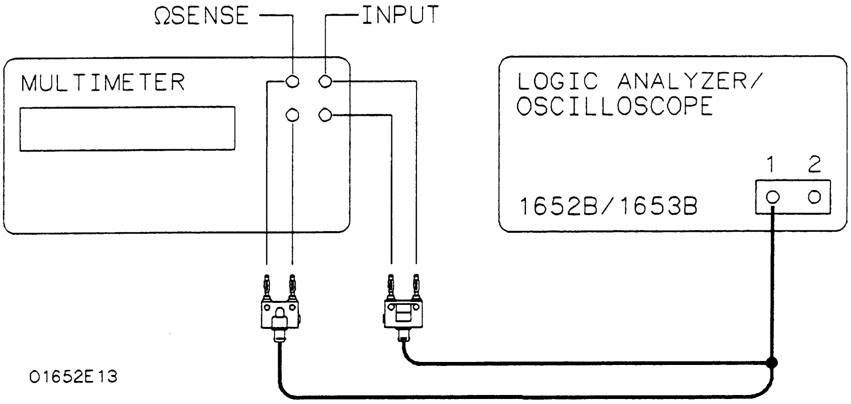
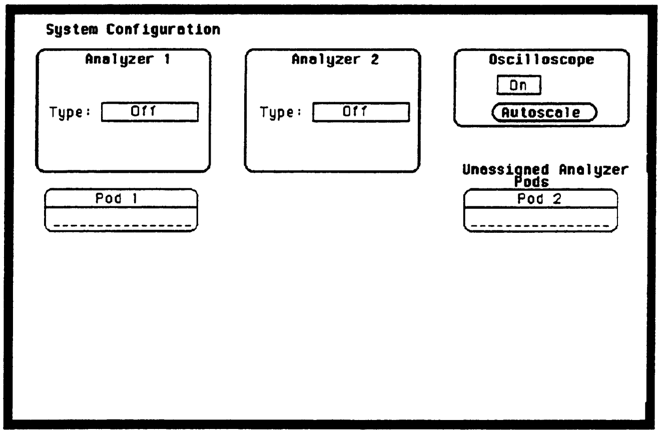


Figure 3-41. Setup for Input Resistance Test

3. Connect the male end of the BNC tee to the channel 1 input of the HP 1652B/1653B oscilloscope.
4. In the **System Configuration** menu, turn both State/Timing Analyzers off and turn the oscilloscope on as in figure 3-42. Refer to steps a through d if you are unfamiliar with menus.



System Configuration

Analyzer 1
Type: Off

Analyzer 2
Type: Off

Oscilloscope
On
Autoscale

Pod 1

Unassigned Analyzer Pods
Pod 2

Figure 3-42. System Configuration for Input Resistance

   a. Move the cursor to the **Type** field of **Analyzer 1** and press the SELECT key.
   b. Set the analyzer **Type** to **Off** using the cursor and SELECT key.
   c. Repeat steps a and b for **Analyzer 2**.
   d. Move the cursor to the **On/Off** field of the **Oscilloscope** and press the SELECT key to turn the oscilloscope **On**.

5. Press the TRACE/TRIG key and use the cursor and SELECT key to set the **Run Mode** to **Single**.
6. Press the FORMAT/CHAN key and use the cursor and SELECT key to set **Input** to **CH 1**.
7. Set the **Impedance** to **1 MOhm** and press RUN. The multimeter should read 1 MΩ ±10 kΩ.
8. Set the **Impedance** to **50 Ohms** and press RUN. The multimeter should read 50 Ω ±0.5 Ω.
9. Repeat steps 3, 6, 7, and 8 for channel 2.

Note

Failure of this test indicates a faulty attenuator if resistance is out of specifications. The oscilloscope assembly also may be at fault if input resistance cannot be changed. See troubleshooting in section 6C for more information.

Voltage Measurement Accuracy Test

Description:

This test verifies the voltage measurement accuracy of the instrument.

Specification:

± (Gain Accuracy + Offset Accuracy + ADC Resolution)

Equipment Required:

Power Supply	HP 6114A
Digital Multimeter	HP 3478A
BNC Cable	HP 10503A
BNC (f)-to-Banana (m) Adapter	HP 1251-2277
Banana (m)-to-Banana (m) Cable (2)	HP 11000-60001

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-43.

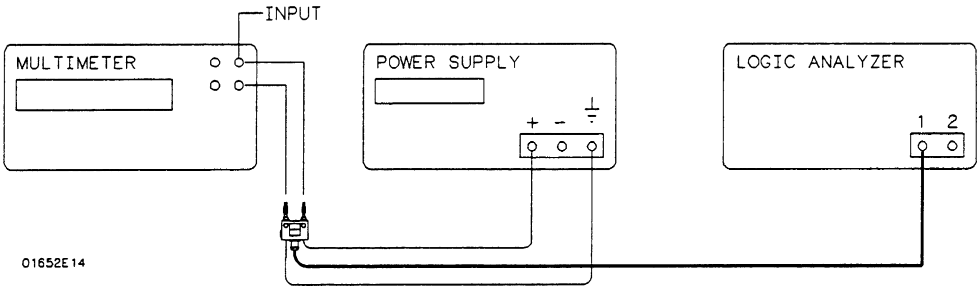
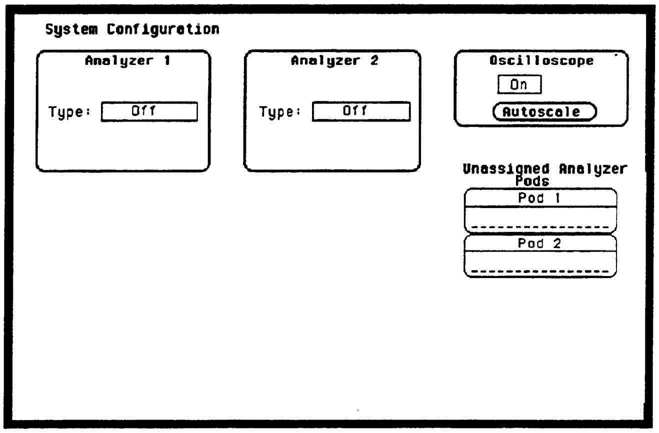


Figure 3-43. Setup for Voltage Measurement Accuracy

2. Connect the power supply to Channel 1 of the HP 1652B/1653B oscilloscope.
3. In the **System Configuration** menu, turn both State/Timing Analyzers off and turn the oscilloscope on as shown in the previous test figure 3-42.

4. Unassign all of the pods from the analyzers as shown in figure 3-44. Refer to steps a through c if you are unfamiliar with menus.


System Configuration

Analyzer 1

Type: Off

Analyzer 2

Type: Off

Oscilloscope

On

Unassigned Analyzer Pods

Pod 1

Pod 2

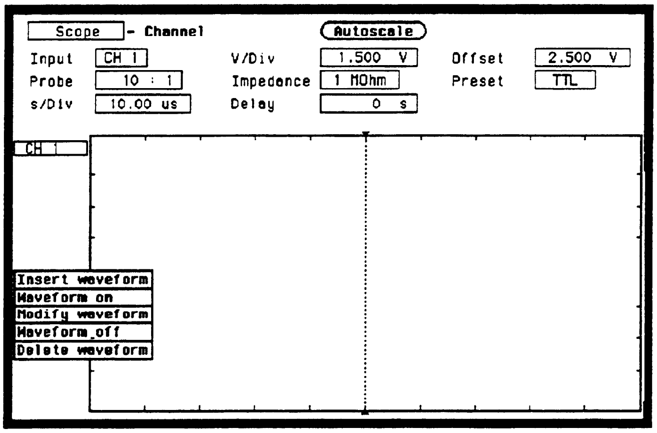
Figure 3-44. System Configuration

a. Move the cursor to an assigned pod and press SELECT.

b. Move the cursor to **Unassigned** and press SELECT.

c. Repeat steps a and b for all assigned pods.

5. Press the FORMAT/CHAN key and turn off channel 2 by deleting the channel 2 waveform as in figure 3-45. Refer to steps a and b if you are unfamiliar with menus.


Scope - Channel

Input CH 1

Probe 10 : 1

s/Div 10.00 us

V/Div 1.500 V

Impedance 1 MOhm

Delay 0 s

Offset 2.500 V

Preset TTL

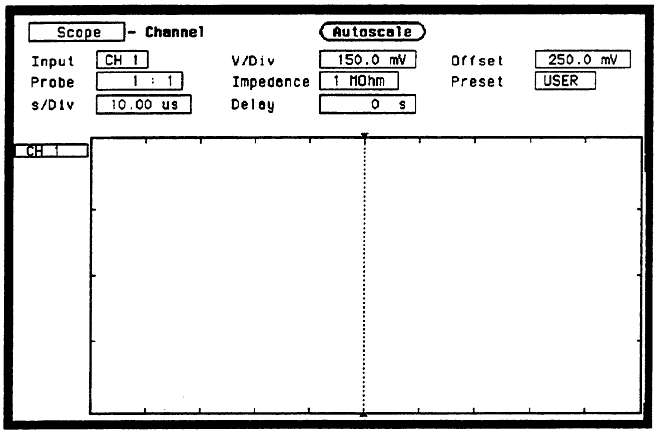
CH 1

Figure 3-45. Deleting Channel 2

a. Move the cursor to **CH 2** at the left side of the display and press SELECT.

b. Move the cursor to **Delete waveform** and press SELECT.

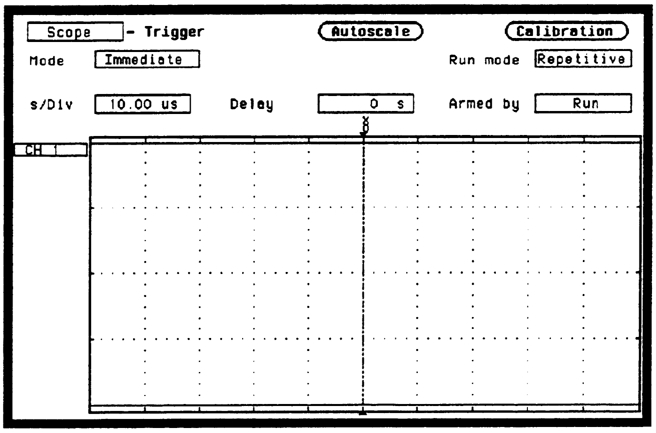
6. Using the knob and SELECT key, set **Input** to **CH 1**, **Probe** to **1:1**, and **Impedance** to **1 MOhm** as in figure 3-46.


Scope
- Channel
Autoscale
CH 1

Input CH 1
V/Div 150.0 mV
Offset 250.0 mV
Probe 1 : 1
Impedance 1 MOhm
Preset USER
s/Div 10.00 us
Delay 0 s

Figure 3-46. Channel Menu Configuration

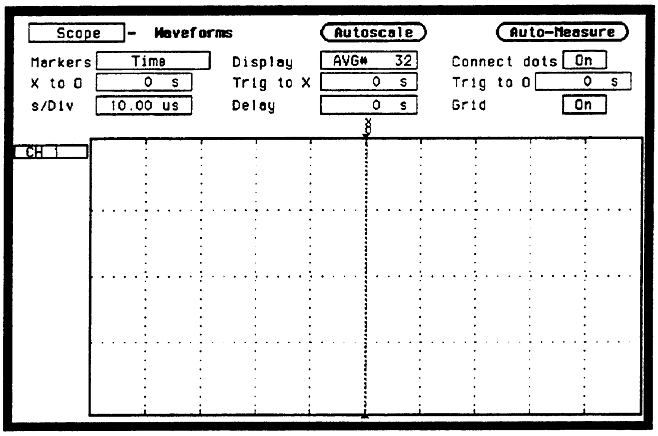
7. Press the TRACE/TRIG key and set the **Mode** to **Immediate** and **Run mode** to **Repetitive** as in figure 3-47.


Scope
- Trigger
Autoscale
Calibration
CH 1

Mode Immediate
Run mode Repetitive
s/Div 10.00 us
Delay 0 s
Armed by Run

Figure 3-47. Trigger Menu Configuration

8. Press DISPLAY and set **Markers** to **Time**, **Display** to **AVG# 32**, **Connect dots** to **On**, and **Grid** to **On** as in figure 3-48.



Markers Time
X to O 0 s
s/Div 10.00 us
Display AVG# 32
Trig to X 0 s
Delay 0 s
Connect dots On
Trig to O 0 s
Grid On

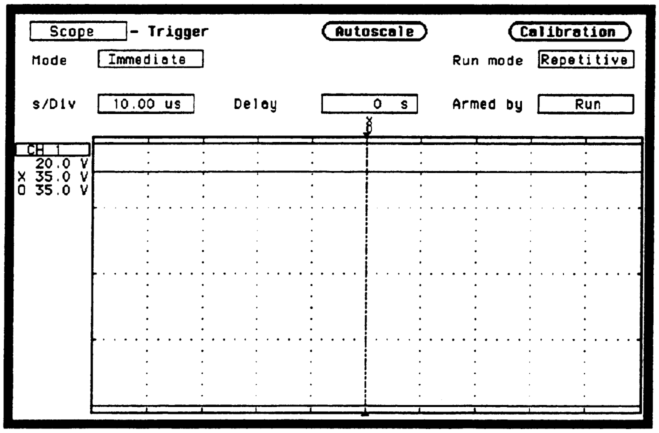
Figure 3-48. Waveforms Menu Configuration

9. Press the FORMAT/CHAN key and set **V/Div** and **Offset** according to the first line of the following table.

V/Div	Offset	Power Supply	Test Tolerance	X and O Result
10.0 V	20.00 V	35.0 V	±3.242 V	31.758 - 38.242 V
5.0 V	10.00 V	17.5 V	±1.622 V	15.878 - 19.122 V
2.0 V	4.00 V	7.0 V	±0.650 V	6.935 - 7.065 V
1.0 V	2.00 V	3.5 V	±0.326 V	3.174 - 3.826 V
500 mV	1.00 V	1.75 V	±0.164 V	1.586 - 1.914 V
200 mV	400 mV	700 mV	±66.8 mV	633.2 - 766.8 mV
100 mV	200 mV	350 mV	±34.4 mV	315.6 - 384.4 mV
50 mV	100 mV	175 mV	±18.2 mV	156.8 - 193.2 mV
20 mV	40 mV	70 mV	±8.48 mV	61.52 - 78.48 mV
15 mV	30 mV	50 mV	±6.86 mV	43.14 - 56.86 mV

10. Set the power supply to the voltage listed on the first line of the previous table.

11. Press the TRACE/TRIG key, then press RUN. The Trigger level cursor will appear as in figure 3-49.



```
Scope - Trigger
Mode      Immediate                       Run mode   Repetitive
s/Div     10.00 us     Delay     0 s      Armed by   Run
CH 1
  20.0 V
X 35.0 V
O 35.0 V
```

Figure 3-49. Trigger Menu

12. After the display has time to settle, observe the X and O cursor voltage display. Verify that these voltages are within the limits in the previous table and press STOP.

13. Repeat steps 9 through 12 for each line of the table.

14. Press the FORMAT/CHAN key and turn on channel 2 by inserting a waveform on the display. Refer to steps a through c if you are unfamiliar with menus.

    a. Move the cursor to **CH 1** at the left side of the display and press SELECT.

    b. Move the cursor to **Insert waveform** and press SELECT.

    c. Move the cursor to **CH 2** and press SELECT.

15. Turn off channel 1 by deleting the channel 1 waveform.

16. Set **Input** to **CH 2** and connect the power supply to Channel 2.

17. Repeat steps 6 through 13 for channel 2.

Note

Voltage measurement errors can be caused by the need for self-calibration. Perform the **Offset Calibration** and **Gain Calibration** (see Adjustments, section 4) before troubleshooting the instrument. If self-calibration fails to correct the problem, the cause may be the attenuator or the oscilloscope assembly.

DC Offset Accuracy Test

Description:

This test verifies the DC offset accuracy of the instrument.

Specification:

±(2 mV + 2% of channel offset + 2.5% of full scale)

Equipment Required:

Digital Voltmeter	HP 3478A
Power Supply	HP 6114A
BNC Cable	HP 10503A
BNC (f)-to-Banana (m) Adapter	HP 1251-2277
Banana (m)-to-Banana (m) Cable	HP 11000-60001

Procedure:

1. Connect the HP 1652B/1653B and test equipment as in figure 3-50.

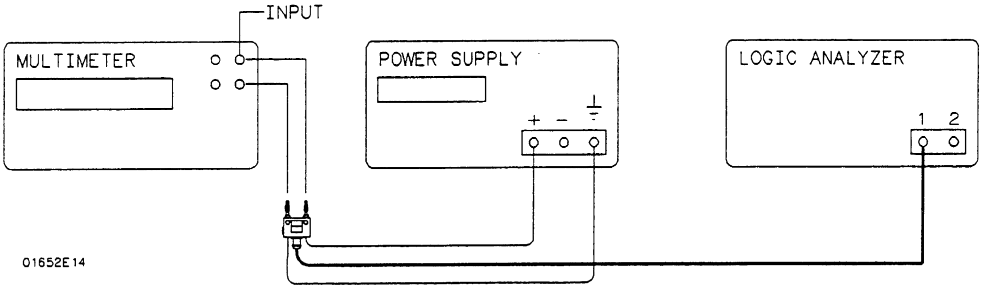


Figure 3-50. Setup for DC Offset Accuracy

2. In the **System Configuration** menu, turn both State/Timing Analyzers off, unassign all of the pods from the analyzers, and turn the oscilloscope on as in the previous test figure 3-44.

3. Press the FORMAT/CHAN key and turn on channel 1 by inserting the channel 1 waveform. Then turn off channel 2 by deleting the channel 2 waveform.

4. Using the knob and SELECT key, set **Input** to **CH 1**, **Probe** to **1:1**, and **Impedance** to **1 MOhm** as in the previous test figure 3-46.

5. Press the TRACE/TRIG key and set the **Mode** to **Immediate** and the **Run mode** to **Repetitive** as in figure 3-51.

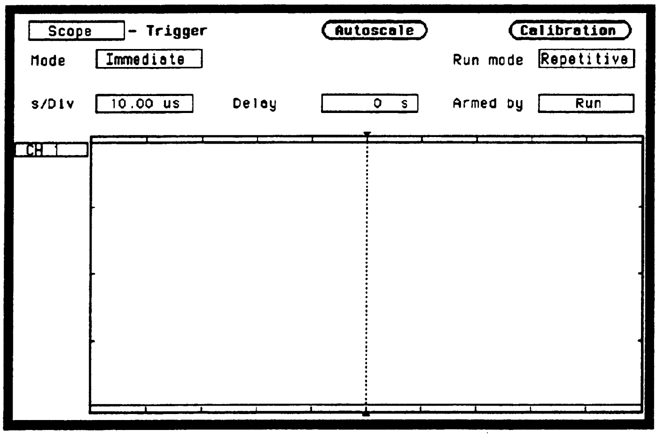

Scope - Trigger
Mode Immediate
Run mode Repetitive
s/Div 10.00 us
Delay 0 s
Armed by Run

Figure 3-51. Trigger Menu

6. Press DISPLAY and set the **Markers** to **Time**, **Display** to **AVG# 32**, **Connect dots On**, and **Grid On** as in figure 3-52.

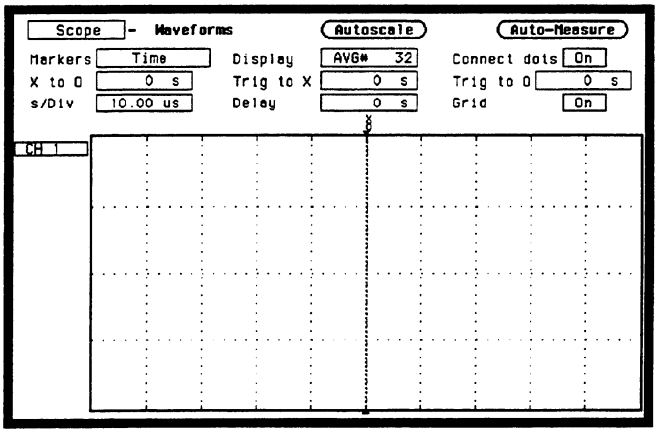

Scope - Waveforms
Markers Time
X to O 0 s
s/Div 10.00 us
Display AVG# 32
Trig to X 0 s
Delay 0 s
Connect dots On
Trig to O 0 s
Grid On

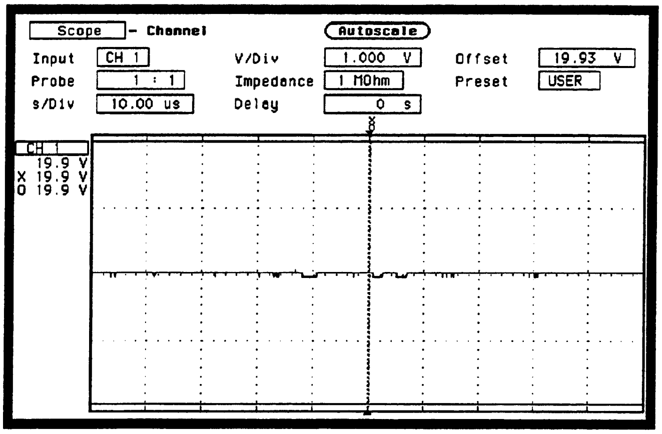
Figure 3-52. Waveforms Display Menu

7. Press FORMAT/CHAN and set **V/Div** and **Offset** according to the first line of the following table.

V/Div	Offset	Power Supply	Test Tolerance	Offset Result
1.0 V	20.0 V	20.0 V	±0.502 V	19.50 - 20.50 V
500 mV	10.0 V	10.0 V	±0.242 V	9.758 - 10.242 V
200 mV	5.0 V	5.0 V	±0.122 V	4.878 - 5.122 V
100 mV	2.0 V	2.0 V	±0.052 V	1.948 - 2.052 V

8. Set the power supply to the voltage listed on the first line of the previous table.

9. Press RUN and readjust **Offset** so the trace is as close to the center horizontal line of the graticule as possible after it has settled (averaging complete) as in figure 3-53.



Input CH 1
Probe 1 : 1
s/Div 10.00 us
V/Div 1.000 V
Impedance 1 MOhm
Delay 0 s
Offset 19.93 V
Preset USER

CH 1
19.9 V
X 19.9 V
O 19.9 V

Figure 3-53. Channel Menu

10. Verify that the **Offset** voltage is within the limits specified in the previous table. Then press STOP.

11. Repeat steps 7 through 10 for each line of the table.

12. Turn on channel 2 by inserting a waveform on the display. Refer to steps a through c if you are unfamiliar with menus.

    a. Move the cursor to **CH 1** at the left side of the display and press SELECT.

    b. Move the cursor to **Insert waveform** and press SELECT.

    c. Move the cursor to **CH 2** and press SELECT.

13. Turn off channel 1 by deleting the channel 1 waveform.

14. Set **Input** to **CH 2** and connect the power supply to Channel 2.

17. Repeat steps 7 through 11 for channel 2.

Note

Offset errors can be caused by the need for self-calibration. Perform the **Offset Calibration** (see Adjustments) before troubleshooting the instrument. If self-calibration fails to correct the problem, the cause may be the attenuator or oscilloscope assembly.

Bandwidth Test

Description:

This test checks the bandwidth of the oscilloscope in the HP 1652B/1653B.

Note Before doing the Bandwidth test, verify that the **Attenuator Calibration** is valid (performed within the last six months or 1000 hours).

Specification:

Bandwidth: dc to 100 MHz

Equipment Required:

Signal Generator	HP 8656B
Power Meter	HP 436A
Power Sensor	HP 8482A
Power Splitter	HP 11667B
Type N (m) 24 inch cable	HP 11500B
Type N (m) to BNC (m) Adapter	HP 1250-0082

Procedure:

1. With the N cable, connect the signal generator to the power splitter input. Connect the power sensor to one output of the power splitter as in figure 3-54.

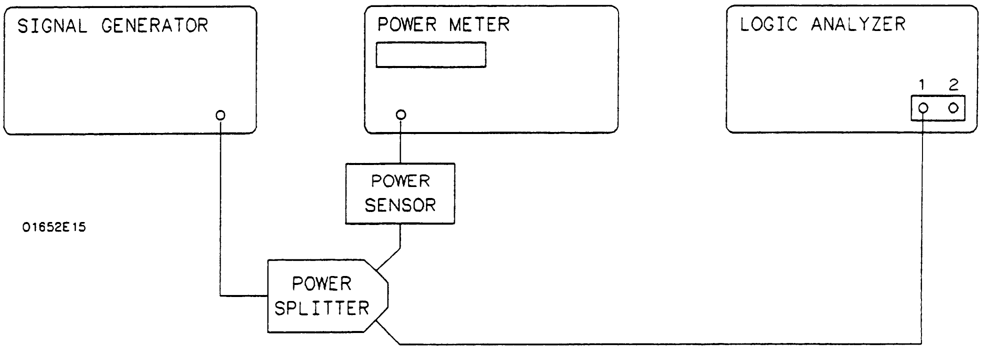


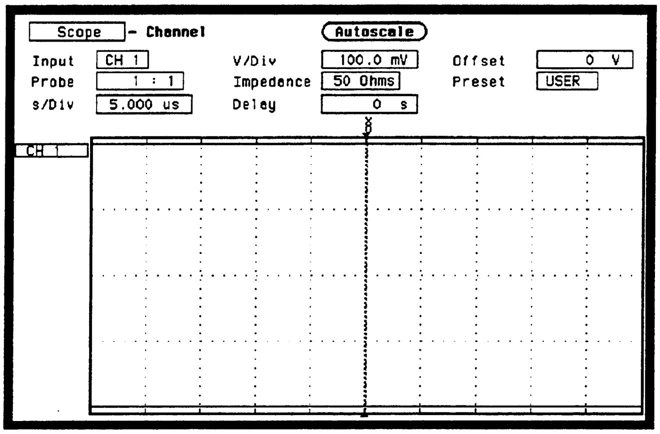
Figure 3-54. Setup for Bandwidth Test

2. Using an N-to-BNC adapter, connect the other power splitter output to the channel 1 input of the HP 1652B/1653B oscilloscope.

3. In the **System Configuration** menu, turn both State/Timing Analyzers off, unassign all of the pods from the analyzers, and turn the oscilloscope on as in the previous figure 3-44.

4. Press FORMAT/CHAN and turn on channel 1 by inserting the channel 1 waveform. Then turn off channel 2 by deleting the channel 2 waveform.

5. Set the **Input** to **CH 1**, **V/Div** to **100 mV**, **Offset to 0 V**, **Probe** to **1:1**, **Impedance** to **50 Ohms**, and **s/Div** to **5.0 us** as in figure 3-55.



Scope - Channel

Input CH 1

Probe 1 : 1

s/Div 5.000 us

V/Div 100.0 mV

Impedance 50 Ohms

Delay 0 s

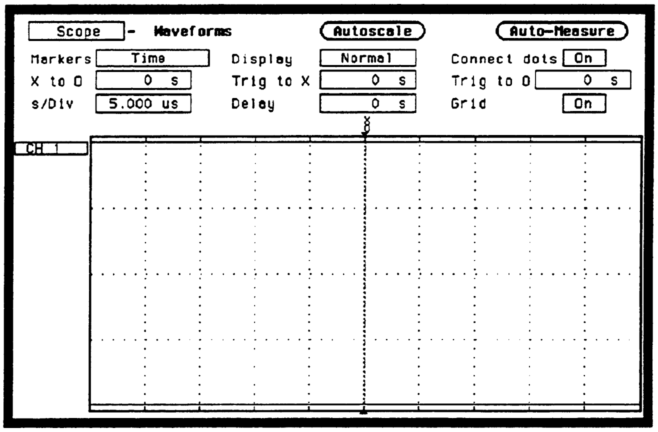
Offset 0 V

Preset USER

Figure 3-55. Channel Menu Configuration

6. Press TRACE/TRIG and set the **Run mode** to **Repetitive** and trigger **Level** to **0 V** as in the previous figure 3-51.

7. Press DISPLAY and set **Markers** to **Time**, **Display** to **Normal**, **Connect dots On**, and **Grid On** as in figure 3-56.



Scope - Waveforms

Markers Time

X to O 0 s

s/Div 5.000 us

Display Normal

Trig to X 0 s

Delay 0 s

Connect dots On

Trig to O 0 s

Grid On

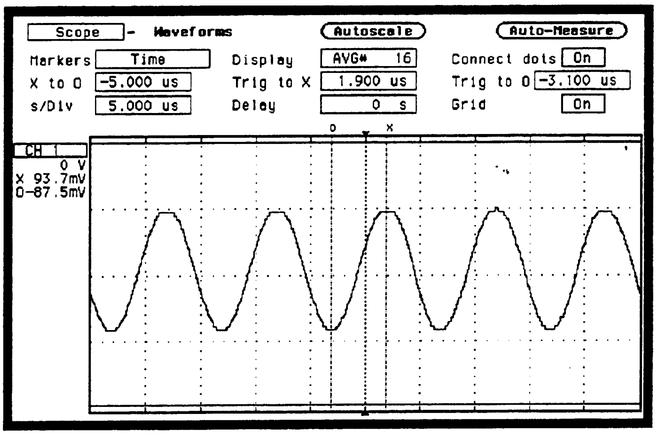
Figure 3-56. Waveforms Display Menu Configuration

8. Set the signal generator for 100 kHz at -4.5 dBm and press RUN on the HP 1652B/1653B. The signal on screen should be five cycles at two divisions amplitude.

9. Press TRACE/TRIG and adjust the trigger **Level** for a stable display. The signal on screen should be five cycles at approximately 2 divisions amplitude.

10. Press DISPLAY and set **Display** to **AVG# 16**.

11. After the measurement settles (averaging complete, about 10 seconds) use **Auto-Measure** to obtain a peak-to-peak voltage measurement as in figure 3-57.



Markers Time
X to O -5.000 us
s/Div 5.000 us
Display AVG# 16
Trig to X 1.900 us
Delay 0 s
Connect dots On
Trig to O -3.100 us
Grid On

0 V
X 93.7mV
O-87.5mV

Figure 3-57. Waveforms Display Menu

12. Set the power meter Cal Factor % to the 100 kHz value from the cal chart on the power sensor probe, then press dB[REF] to set a 0 dB reference.

13. In the Waveforms Display menu, set **Display** to **Normal and s/Div** to **5 ns.**

14. Change the signal generator to 100 MHz and set the power meter Cal Factor to the 100 MHz % value from chart.

15. Adjust the signal generator amplitude for a power reading as close as possible to 0.0 dB(REL).

16. Set the oscilloscope **Display** to **AVG# 16.**

17. After the measurement settles (averaging complete), use **Auto-Measure** to obtain a peak-to-peak voltage as in step 11. Note this value.

18. Calculate the response using the formula:

$$\text{Response (dB)} = 20 \log_{10} \frac{V_{100\text{MHz}}}{V_{100\text{kHz}}}$$

19. Correct the result from step 18 with any difference in the power meter from step 15. Observe signs. For example:

Result from step 18 = -2.3 dB

Power meter reading = -0.2 dB(REL)

true response = (-2.3)-(-0.2) = -2.1 dB

20. Turn on channel 2 by inserting a waveform on the display.

21. Turn off channel 1 by deleting the channel 1 waveform.

22. Connect the power splitter to channel 2 and repeat steps 5 through 19 for channel 2.

Note Failure of the bandwidth test can be caused by faulty attenuator or oscilloscope assembly, or the need for high-frequency pulse response adjustment.

Time Measurement Accuracy Test

Description:

This test uses a precise frequency source to check the accuracy of the time measurement functions.

Specification:

± (500 ps + 2% X s/Div + 0.01% X delta-t)

Equipment Required:

Signal Generator	HP 8656B
BNC Cable	HP 10503A
Type N (m) to BNC (f) Adapter	HP 1250-0780

Procedure:

1. Use a Type N to BNC adapter to connect the signal generator to the channel 1 input of the HP 1652B/1653B oscilloscope as in figure 3-58.

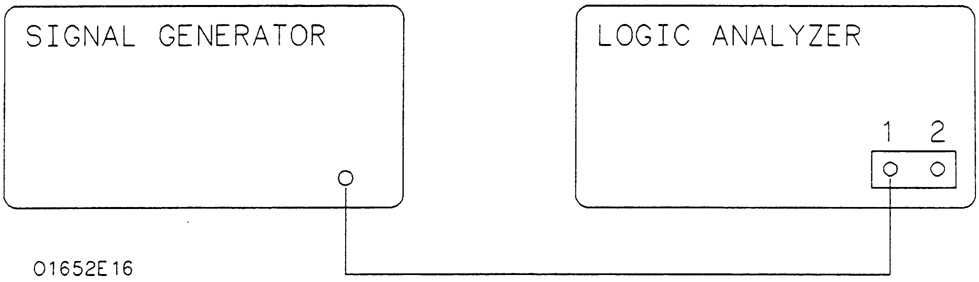
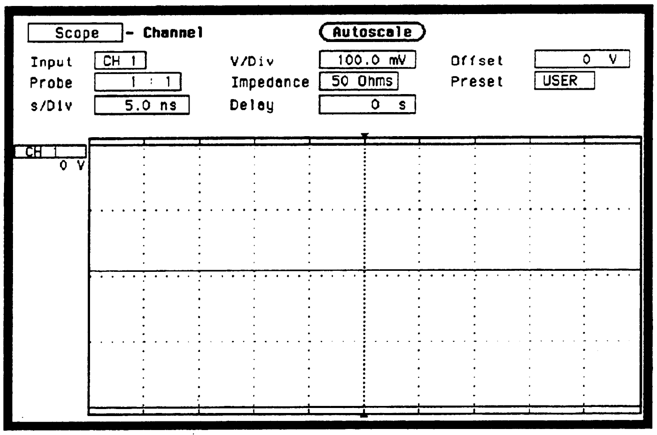


Figure 3-58. Setup for Time Measurement Accuracy

2. In the **System Configuration** menu, turn both State/Timing Analyzers off, unassign all of the pods from the analyzers, and turn the oscilloscope on as in the previous figure 3-44.

3. Press FORMAT/CHAN and turn on channel 1 by inserting the channel 1 waveform. Then turn off channel 2 by deleting the channel 2 waveform.

4. Set **Input** to **CH 1, V/Div** to **100 mV, Offset** to **0 V, Probe** to **1:1, Impedance** to **50 Ohms**, and **s/Div** to **5.0 ns** as in figure 3-59.



Input CH 1
Probe 1 : 1
s/Div 5.0 ns
V/Div 100.0 mV
Impedance 50 Ohms
Delay 0 s
Offset 0 V
Preset USER
CH 1 0 V

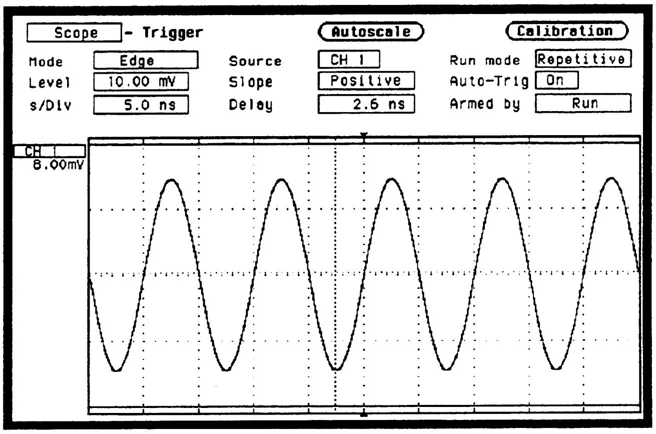
Figure 3-59. Channel Menu Configuration

5. Press DISPLAY and set **Display** to **Normal, Connect dots On**, and **Grid On.**

6. Press TRACE/TRIG and set the **Run mode** to **Repetitive** and trigger **Level** to **0 V** as in the previous figure 3-51.

7. Set the signal generator to 100 MHz at approximately 150 mV.

8. Press RUN and use the **Level** and **Delay** to center the rising edge of the waveform as close as possible to center screen as in figure 3-60. It may be necessary to use **Offset** to center the signal symmetrically about the horizontal axis.



Mode Edge
Level 10.00 mV
s/Div 5.0 ns
Source CH 1
Slope Positive
Delay 2.6 ns
Run mode Repetitive
Auto-Trig On
Armed by Run
CH 1 8.00mV

Figure 3-60. Centering the Waveform

9. Press STOP, then press DISPLAY. Set **Display** to **AVG# 16.**

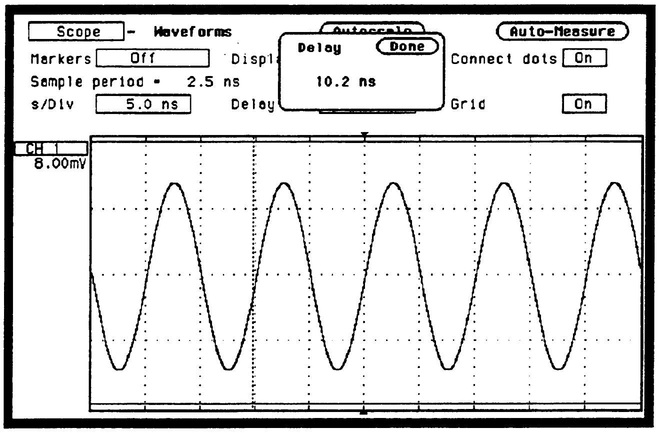
10. Press RUN and when the waveform has stabilized at center screen, press STOP.

11. Use the following table for the next steps.

Delay	Tolerance	Limits
10 ns	±0.601 ns	9.399 to 10.601 ns
100 ns	±0.610 ns	99.39 to 100.61 ns
500 ns	±0.650 ns	499.35 to 500.65 ns

12. Select Delay and enter the delay value listed on the first line of the previous table using the keypad.

13. Select Delay again and use the knob to move the rising edge of the waveform directly over the center reference as in figure 3-61. Verify that the delay is within the limits specified in the table.



Markers Off
Sample period = 2.5 ns
s/Div 5.0 ns
Delay 10.2 ns
Connect dots On
Grid On

Figure 3-61. Waveforms Display

14. Repeat steps 12 and 13 for the other delays in the table.

15. Set the signal generator to 1 MHz.

16. Press DISPLAY and set Display to Normal.

17. Press FORMAT/CHAN and set **s/Div** to **500 ns** and **Offset** to **0 V.**

18. Repeat steps 8 through 14 using the values in the following table.

Delay	Tolerance	Limits
1 us	±10.600 ns	989.4 to 1.010 us
2 us	±10.700 ns	1.989 to 2.010 us

19. Turn on channel 2 by inserting a waveform on the display.

20. Turn off channel 1 by deleting the channel 1 waveform.

21. Connect the signal generator to channel 2 and repeat steps 4 through 18 for channel 2.

Note Time Measurement Accuracy failure is caused by a defective oscilloscope assembly.

Trigger Sensitivity Test

Description:

This test checks the channel trigger for sensitivity at the rated bandwidth.

Note Before doing the Trigger Sensitivity test, verify that the **Trigger Calibration** is valid (performed in the last 6 months or 1000 hours).

Specification:

10.0% of full scale.

Equipment Required:

Signal Generator	HP 8656B
BNC Cable	HP 10503A
Type N (m)-to-BNC (f)	HP 1250-0780

Procedure:

1. Use the Type N-to-BNC adapter to connect the signal generator to channel 1 of the HP 1652B/1653B as in figure 3-62.

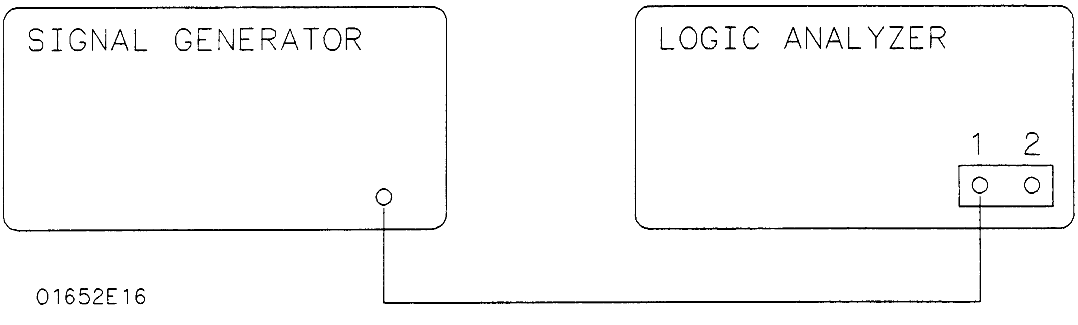
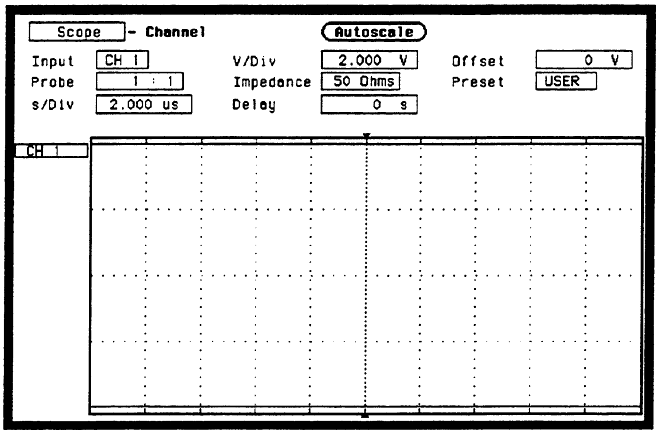


Figure 3-62. Setup for Trigger Sensitivity

2. In the **System Configuration** menu, turn both State/Timing Analyzers off, unassign all of the pods from the analyzers, and turn the oscilloscope on as in the previous figure 3-44.

3. Press FORMAT/CHAN and turn on channel 1 by inserting the channel 1 waveform. Then turn off channel 2 by deleting the channel 2 waveform.

4. Set **Input** to **CH 1**, **V/Div** to **2 V**, **Offset** to **0 V**, **Probe** to **1:1**, **Impedance** to 50 **Ohms**, and **s/Div** to **2.0 us** as in figure 3-63.


Scope - Channel

Input CH 1

Probe 1 : 1

s/Div 2.000 us

V/Div 2.000 V

Impedance 50 Ohms

Delay 0 s

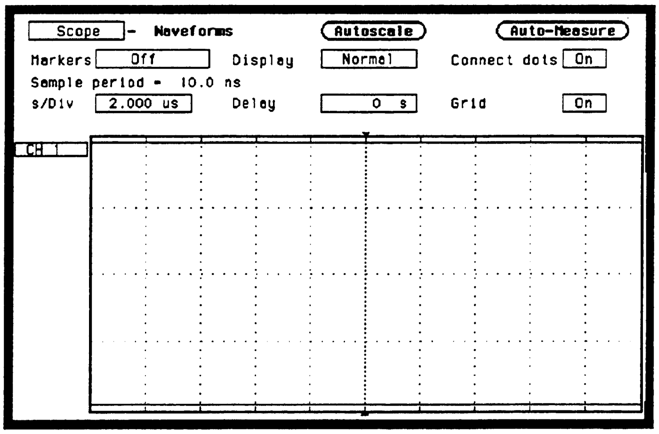
Offset 0 V

Preset USER

Figure 3-63. Channel Menu Configuration

5. Press TRACE/TRIG and set the **Run mode** to **Repetitive** and trigger **Level** to **0 V.**

6. Press DISPLAY and set **Display** to **Normal**, **Connect dots On**, and **Grid On** as in figure 3-64.


Scope - Waveforms

Markers Off

Sample period = 10.0 ns

s/Div 2.000 us

Display Normal

Delay 0 s

Connect dots On

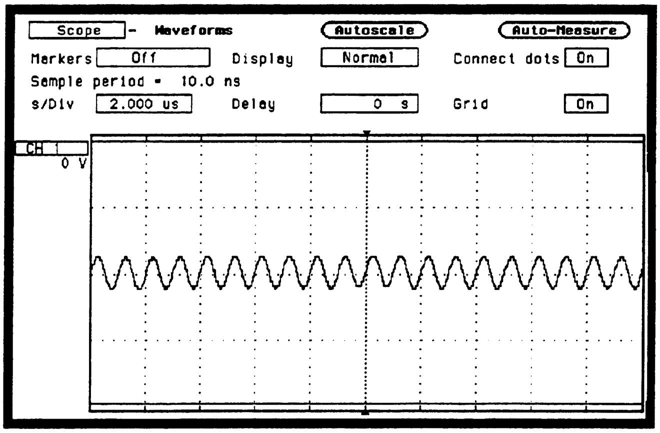
Grid On

Figure 3-64. Waveforms Display Menu

7. Set the signal generator to 1 MHz and press RUN on the HP 1652B/1653B.

8. Adjust the signal generator output level for 0.4 divisions of vertical deflection (approximately +3 dBm).

9. Press TRACE/TRIG and adjust the trigger **Level** for a stable display (Auto-triggered message does not appear on screen). The test passes if triggering is stable, as shown in figure 3-65.



Markers Off Display Normal Connect dots On
Sample period = 10.0 ns
s/Div 2.000 us Delay 0 s Grid On
0 V

Figure 3-65. Waveforms Display Menu

10. Press STOP and set the **s/Div** to **5 ns**.
11. Set the signal generator to 100 MHz and press RUN on the HP 1652B/1653B.
12. Adjust the signal generator output level for 0.4 divisions of vertical deflection (approximately +3 dBm).
13. Press TRACE/TRIG and adjust the trigger level for a stable display (Auto-triggered message does not appear on screen). The test passes if triggering is stable.
14. Press FORMAT/CHAN and set V/Div to 200 mV and repeat steps 4 through 13. The signal generator output should be reduced to approximately -17 dBm.
15. Press FORMAT/CHAN and set V/Div to 20 mV and repeat steps 4 through 13. The signal generator output should be set to approximately -37 dBm.
16. Turn on channel 2 by inserting a waveform on the display.
17. Turn off channel 1 by deleting the channel 1 waveform.
18. Connect the signal generator to channel 2 and repeat steps 4 through 15 for channel 2.

Note Trigger sensitivity test failure is caused by a defective attenuator or oscilloscope assembly.

Table 3-1. Performance Test Record

Hewlett-Packard Model 1652B/1653B Logic Analyzer Serial Number ____________	Tested by ____________ Work Order No. ________ Date Tested ____________

Recommended Calibration
Interval _24_ Months

Test	Results		
Clock, Qualifier, and Data Inputs Test 1		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 2		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 3 (HP 1652B Only)		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 4		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Clock, Qualifier, and Data Inputs Test 5		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____

Table 3-1. Performance Test Record (continued)

Test	Results		
Clock, Qualifier, and Data Inputs Test 6		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Glitch Test		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____
Threshold Accuracy Test		Passed	Failed
	Pod1	_____	_____
	Pod2	_____	_____
	Pod3	_____	_____
	Pod4	_____	_____
	Pod5	_____	_____

Table 3-1. Performance Test Record (continued)

Test	Limits		Results	
Voltage Measurement Accuracy Test	Range		Chan 1	Chan2
	10.0 V	31.758 - 38.242 V	______	______
	5.0 V	15.878 - 19.122 V	______	______
	2.0 V	6.935 - 7.065 V	______	______
	1.0 V	3.174 - 3.826 V	______	______
	500 mV	1.586 - 1.914 V	______	______
	200 mV	633.2 - 766.8 mV	______	______
	100 mV	315.6 - 384.4 mV	______	______
	50 mV	156.8 - 193.2 mV	______	______
	20 mV	61.52 - 78.48 mV	______	______
	15 mV	43.14 - 56.86 mV	______	______
DC Offset Accuracy Test	Range		Chan 1	Chan 2
	1.0 V	19.50 - 20.50 V	______	______
	500 mV	9.758 - 10.242 V	______	______
	200 mV	4.878 - 5.122 V	______	______
	100 mV	1.948 - 2.052 V	______	______
Bandwidth Test			Chan 1	Chan 2
		Down <3dB at 100 MHz	_____	_____
Time Measurement Accuracy Test			Chan 1	Chan 2
	10 ns	9.4 to 10.6 ns	______	______
	100 ns	99.4 to 100.6 ns	______	______
	500 ns	499.4 to 500.6 ns	______	______
	1 us	989.5 to 1.010 us	______	______
	2 us	1.990 to 2.010 us	______	______
Trigger Sensitivity Test			Chan 1	Chan 2
	2 V/div	0.4 div at 1 MHz	______	______
		0.4 div at 100 MHz	______	______
	200 mV/div	0.4 div at 1 MHz	______	______
		0.4 div at 100 MHz	______	______
	20 mV/div	0.4 div at 1 MHz	______	______
		0.4 div at 100 MHz	______	______

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4

Adjustments and Calibration

Introduction

This section provides the adjustment procedures for the HP 1652B/1653B. The primary adjustments groups are:

- Power Supply Assembly Adjustment.
- CRT Monitor Assembly Adjustment.
- System Board Assembly Threshold Adjustment.
- Oscilloscope Assembly High-Frequency Pulse Adjustment.

This section also contains the software calibration procedures for the oscilloscope assembly.

Caution

The effects of ELECTROSTATIC DISCHARGE can damage electronic components. Use grounded wriststraps and mats when performing any kind of service to this instrument.

Equipment Required

The equipment required for the adjustments and calibration procedures in this section are listed in the Recommended Equipment table in section 1 of this manual. Any equipment that satisfies the critical specifications listed in this table may be substituted for the recommended model. Equipment for individual procedures is listed with the procedure.

Adjustments and Calibration Interval

The recommended adjustment interval for the HP 1652B/1653B is two years. The adjustments are set at the factory on assemblies when they are tested. However, adjustments may be necessary after repairs have been made to the instrument. Usually the only assembly that may require adjustments is the assembly that has been replaced.

Warning

Read the Safety Summary at the beginning of this manual before performing any adjustment procedures.

Software calibration should be done on the HP 1652B/1653B oscilloscope under any of the following conditions:

- At six month intervals or every 1,000 hours.
- If the ambient temperature changes more than 10° C from the temperature at the last software calibration.
- To optimize measurement accuracy.

Safety Requirements

Specific warnings, cautions, and instructions are placed wherever applicable throughout the manual. These must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with them violates safety standards of design, manufacture, and intended use of this instrument. Hewlett-Packard assumes no liability for the failure of the customer to comply with these safety requirements.

Instrument Warm-up

Adjust and calibrate the instrument at it's environmental ambient temperature and after a 15 minute warm-up.

Adjustments

Unless specified elsewhere, each adjustment procedure must be followed in its entirety and in the same sequence shown.

Caution

The adjustment procedures are performed with the top cover of the instrument removed. Take care to avoid shorting or damaging internal parts of the instrument.

Warning

Read the Safety Summary at the beginning of this manual before performing any adjustment procedures.

Calibration

The calibration procedures in this section should be followed in their entirety and in the same sequence shown in this section. The steps in each succeeding procedure assumes that all the previous procedures have been completed in the proper order.

Note

Calibration constants are stored in system memory and not on the Operating System Disk. Therefore, software calibration is not required when a different Operating System Disk is used to boot the instrument on power-up.

Power Supply Assembly Adjustment

Equipment Required:

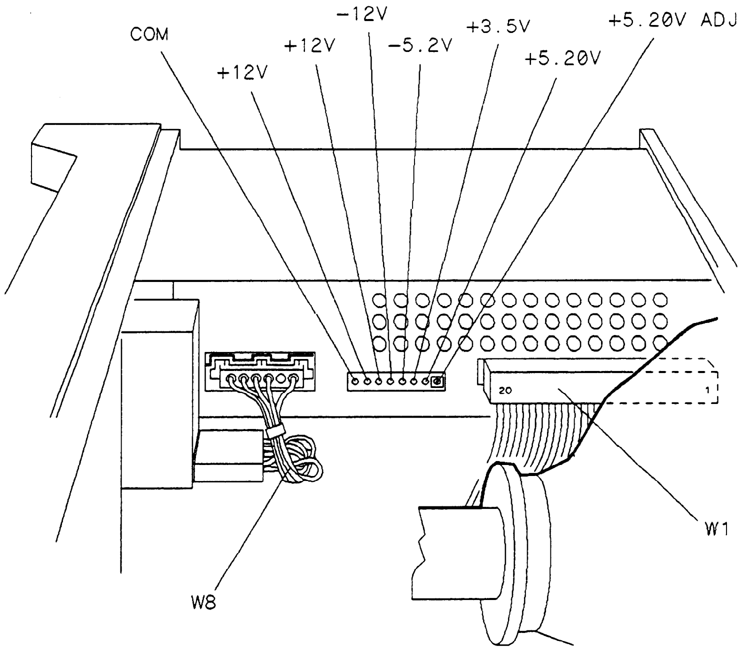
Digital Voltmeter .... HP 3478A

Procedure:

Note The Power Supply Adjustment should be performed prior to the other adjustment and calibration procedures.

---

1. Disconnect the power cord from HP 1652B/1653B and remove the top cover. Then refer to figure 4-1 for the testpoint and adjustment locations.



54502E09

Figure 4-1. Power Supply Adjustments

2. Connect the negative lead of the voltmeter to the COM test point on the Power Supply Assembly.
3. Connect the positive lead of the voltmeter to +5V on the Power Supply Assembly.
4. Connect the power cord to the HP 1652B/1653B and turn the instrument on.
5. The voltmeter reading should be within the range of +5.180 V to +5.220 V. If the voltmeter reading is out of this range, adjust the +5.20V ADJ on the Power Supply Assembly to +5.200 V ±0.020 V (+5.180 V to +5.220 V).

Caution High voltages exist on the sweep board that can cause personal injury. Avoid contact with the CRT monitor sweep board when adjusting the +5.20V.

CRT Monitor Assembly Adjustments

The CRT Monitor Assembly Adjustments optimize the characters of the CRT display. Set up the instrument for these adjustments as follows:

1. Turn off the HP 1652B/1653B and disconnect the power cord. Then remove the top cover.

Caution

The adjustment procedures are performed with the top cover of the instrument removed. Take care to avoid shorting or damaging internal parts of the instrument.

---

2. Connect the power cord to the HP 1652B/1653B and turn on the instrument.
3. In the **System Configuration** menu, select the Type field for Analyzer 1 (MACHINE 1) and, when the pop-up appears, select **Timing**.

Intensity, Sub-Bright, and Contrast Adjustment

1. Press the DISPLAY key to place the **Timing Waveforms** menu on the screen of the HP 1652B/1653B.

Note

This menu is used because it has characters throughout the screen which are watched during the procedures. Any other menu may be used, however, the adjustments may not be as accurate if characters and/or lines are not displayed throughout the screen.

---

2. Set the rear-panel INTENSITY control to its minimum setting.
3. Refer to figure 4-2 for the adjustment locations.

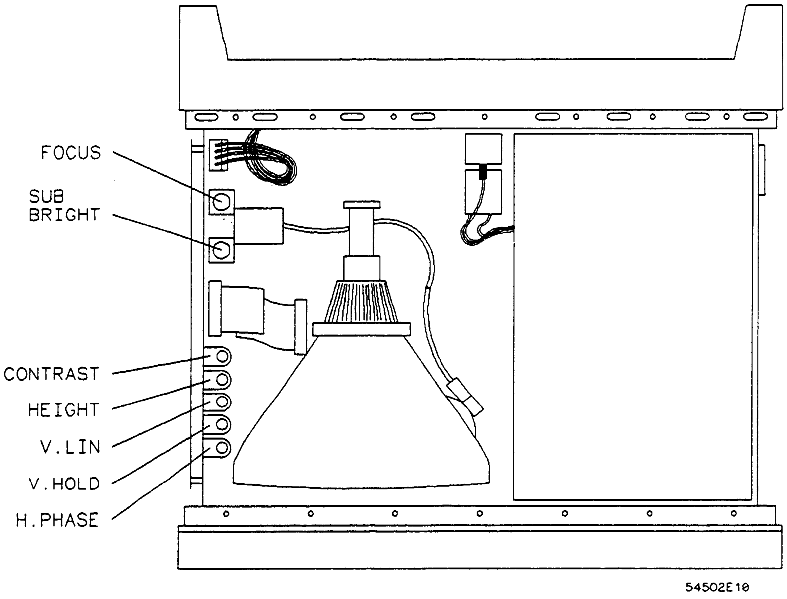


Figure 4-2. CRT Adjustment Locations

4. Adjust the sweep board SUB BRIGHT control to the lowest setting of brightness where the menu is still visible on the CRT screen.

Caution

High voltages exist on the sweep board. Avoid contact with the sweep board when making CRT adjustments.

---

5. Adjust the rear-panel INTENSITY control to bring up the intensity level on screen. Screen intensity should be at a comfortable viewing level and the position of both adjustments should be close to mid-range.

Note

Setting the intensity level excessively high may shorten the life of the CRT. For optimum usage, set the intensity as low as possible while maintaining a comfortable viewing level.

---

6. Press RUN and then STOP.
7. Adjust the sweep board CONTRAST control so that the error message is easily seen.

Focus Adjustment

1. Refer to the previous figure 4-2 for the adjustment locations.
2. Press the DISPLAY key to place the **Timing Waveforms** menu on the screen of the HP 1652B/1653B.
3. Adjust the sweep board FOCUS control for sharp pixels in the center of the screen menu. Then note the FOCUS control position.
4. Adjust the sweep board FOCUS for sharp pixels at the corners of the screen. Then note the FOCUS control position.
5. Set the sweep board FOCUS control for mid-position between the two positions noted in steps 3 and 4 for best over-all pixel focus.

Horizontal Phase, Vertical Linearity, and Height Adjustments

1. Refer to the previous figure 4-2 for adjustment locations.
2. Press DISPLAY to place the **Timing Waveforms** menu on the screen of the HP 1652B/1653B.

Note

This menu is used because it has characters and lines throughout the menu which are watched during the procedures. Any other menu may be used, however, the adjustments may not be as accurate.

---

3. Adjust the sweep board H. PHASE control to center the menu horizontally on the CRT screen.
4. Adjust the sweep board V. LIN control so that the top and bottom rows of text are equal in height. Text height should be approximately 1mm.
5. Adjust the sweep board HEIGHT control so that the screen menu top and bottom borders are equal in width to the side borders of the menu.

6. Readjust steps 4 and 5 as necessary for a uniform display of the screen menu.

Note

The V.LIN and HEIGHT adjustments interact with each other and may need to be repeated for best results.

System Board Assembly Threshold Adjustment

Equipment Required:

Digital Voltmeter	HP 3478A
Power Supply Cable	54503-61604

Procedure:

Note

The threshold adjustment A1R95 is located beneath the oscilloscope board and is not accessible without dismantling part of the instrument. Consequently, it is advisable to see if the threshold requires adjustment before dismantling the instrument. Perform the **Threshold Accuracy Test** in section 3 to verify if adjustment is required before executing this procedure.

1. Disconnect the power cord from HP 1652B/1653B and remove the top cover.
2. Connect the negative (-) lead of the voltmeter to TP GND. Refer to figure 4-3 for testpoint and adjustment locations.

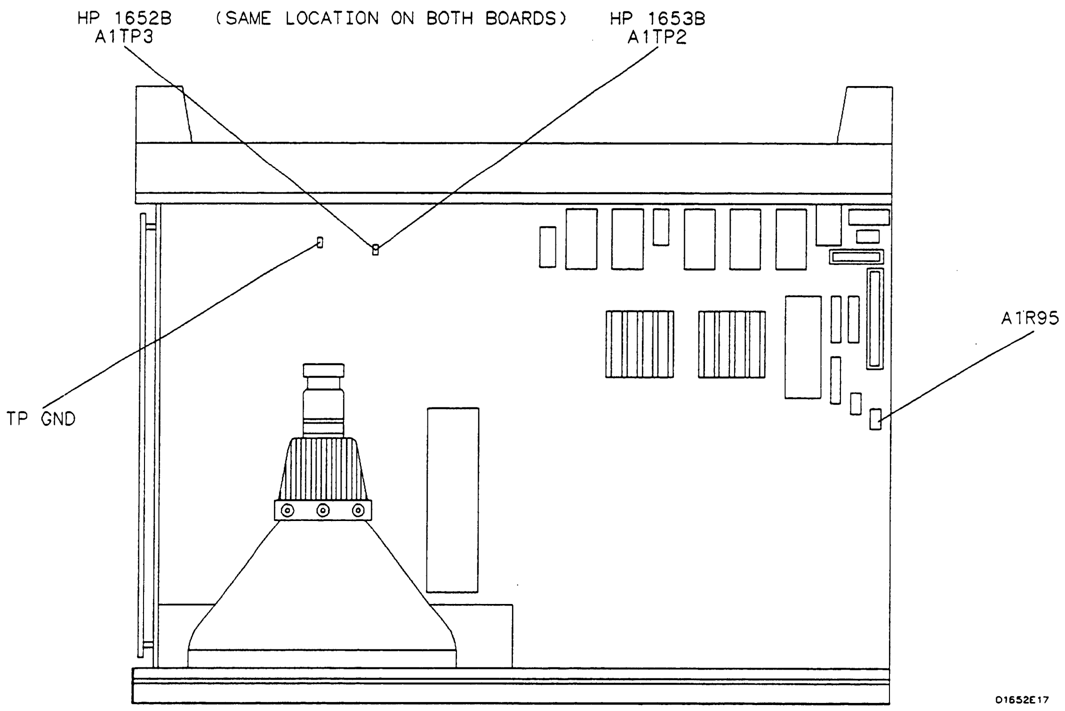


Figure 4-3. System Board Testpoints and Adjustments

3. Connect the positive (+) lead of the voltmeter to A1TP3 on the HP 1652B, or A1TP2 on the HP 1653B, System Board Assembly.

4. Connect the power cord to HP 1652B/1653B and turn on the instrument.

5. Assign pod 3 of the HP 1652B, or pod 2 of the HP 1653B, to a machine in the **System Configuration** menu by using front-panel knob and SELECT key.

6. Press the CHAN/FORMAT key and set the **User-defined** pod threshold of the pod assigned in the previous step to -9.9 V. Refer to the following steps if you are unfamiliar with menus.

   a. Move cursor to the pod threshold field (TTL) with the front-panel knob and press SELECT.

   b. Move the cursor to **User-defined** with the front-panel knob and press SELECT.

   c. Use the front-panel keys to enter the value -9.9 V. Then move the cursor to **Done** and press SELECT.

7. The voltmeter readout should indicate a voltage value within the range of -.975 V to -1.005 V (-.990 V ±0.015 V).

8. Set the **User-defined** pod threshold of the pod assigned in step 6 to +9.9 V.

9. Note voltmeter readout. The voltage reading should be within the range of +.975 V to +1.0005 V (+.990 V ±0.015 V).

10. If either voltage reading is not within the given range, use the following procedure to adjust the threshold level.

    a. Turn off the instrument and disconnect the power cable.

Caution ✋

Never attempt to remove or install any assembly with the instrument ON or the power cable connected. This can result in component damage.

---

   b. Remove the oscilloscope assembly by following the procedure "Removal and Replacement of the Oscilloscope Assembly" in section 6D.

   c. Loosen the two screws that hold the rear bracket on the oscilloscope assembly support panel until the bracket moves freely.

   d. Remove the support panel by carefully tilting the rear of the panel up and lifting the panel out through the top of the instrument cabinet. Make sure the metal tabs on the front of the support panel clear the front panel.

   e. Reconnect the power supply using the power supply cable (HP part number 54503-61604).

   f. Reconnect the disk drive assembly cable to the disk drive.

   g. Reinstall the oscilloscope assembly without the support panel to allow unabstracted access to A1R95.

   h. Reconnect the oscilloscope assembly to the system assembly with the appropriate cable.

i. Reconnect the line filter assembly to the power supply.

j. Reconnect the power cord and turn on the instrument.

k. Repeat steps 5 and 6.

l. Set the **User-defined** pod threshold of the pod assigned to -9.9 V.

m. With the digital voltmeter connected, adjust A1R95 for reading of -.9900 V ±0.0005 V. Refer to figure 4-3 for adjustment locations.

n. Set the **User-defined** pod threshold to +9.9 V.

o. Note the difference between this reading and +0.9900 V.

p. Adjust A1R95 so the difference in step d is halved, ±0.0005 V.

q. When the adjustment is complete, turn off the instrument and remove the power cord. Then reassemble the instrument. Refer to the section "Removal and Replacement of the Oscilloscope Assembly" for addition information on reassembling the instrument.

EXAMPLES

If the reading is + .9952 V, the difference is .0052 V. Adjust A1R95 for +.9926 V ±0.0005 V.

If the reading is + .9834 V, the difference is .0066 V. Adjust A1R95 for +.9867 V ±0.0005 V.

Oscilloscope Assembly High-Frequency Pulse Adjustment

This procedure optimizes the pulse response so that the instrument will meet its bandwidth specification.

Note

This procedure should not be performed as part of the routine adjustments. Typically, it needs to be done only when the instrument fails the bandwidth performance test, an attenuator has been changed, or the oscilloscope assembly has been changed (new combination of attenuators and PC board). Only the channel(s) involved with the failure or repair should be adjusted.

Equipment Required:

Pulse Generator	Picosecond Pulse Labs 2700C
BNC Cable	HP 10503A

Procedures:

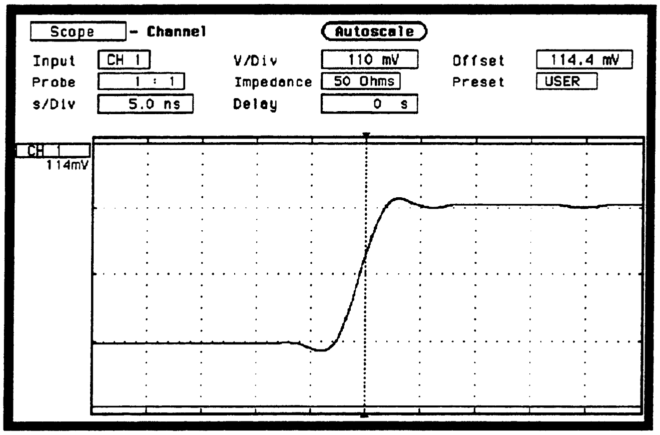
1. Turn off the HP 1652B/1653B and disconnect the power cord. Then remove the top cover.
2. Connect the power cord to the HP 1652B/1653B and turn on the instrument.
3. Set the pulse generator for pulse output.

Caution

Attenuate the signals from the Picosecond Pulse Labs generator by at least 20 dB. Setting the attenuation from 0 dB to 20 dB may result in damage to the HP 1652B/1653B attenuators.

---

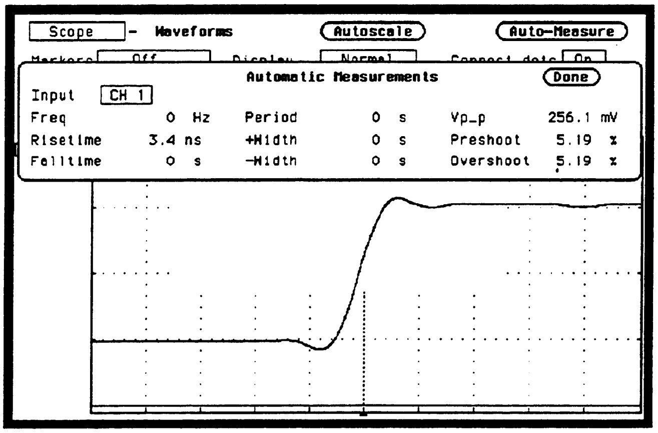
4. In the **System Configuration** menu, turn both State/Timing analyzers Off, and turn the oscilloscope On.
5. Press FORMAT/CHAN and set **V/Div** to **100 mV**, **Offset** to **150 mV**, **Probe** to **1:1**, **Impedance** to **50 Ohms**, and **s/Div** to **5 ns**.
6. Press TRACE/TRIG and set the **Run mode** to **Repetitive**.
7. Press DISPLAY and set **Display** to **Normal**, **Connect dots On**, and **Grid On**.
8. Connect the pulse generator to the channel 1 input of the HP 1652B/1653B oscilloscope and press RUN.
9. Press TRACE/TRIG and adjust the trigger **Level** for a stable display.
10. Press FORMAT/CHAN and adjust **V/Div** and **Offset** to obtain a waveform as shown in figure 4-4.



```
Scope   - Channel                 Autoscale
Input   CH 1          V/Div       110 mV       Offset   114.4 mV
Probe   1 : 1         Impedance   50 Ohms      Preset   USER
s/Div   5.0 ns        Delay       0 s
CH 1
114mV
```

Figure 4-4. Channel Menu

11. Press Display and set **Display** to **AVG# 32.**
12. Select **Auto-Measure** and verify the overshoot and rise time as shown in figure 4-5. Use the SELECT key to toggle the **Auto-Measure** display between CH 1 and CH 2 to update the information.



```
Scope   - Waveforms              Autoscale              Auto-Measure
Markers Off               Display Normal          Connect dots On
                     Automatic Measurements                   Done
Input     CH 1
Freq         0  Hz    Period      0  s     Vp_p       256.1 mV
Risetime   3.4  ns    +Width      0  s     Preshoot    5.19 %
Falltime     0  s     -Width      0  s     Overshoot   5.19 %
```

Figure 4-5. Waveforms Display Menu

13. The rise time should be 3.5 nS and overshoot should be < 10%. If either of these is out of specification, adjust the appropriate capacitor. The capacitor locations are shown in figure 4-6.

    - Capacitor C119 is for Channel 1.
    - Capacitor C161 is for Channel 2.

    These capacitors are located on the oscilloscope assembly board. They can be accessed through the right side of the instrument, just below the power supply assembly. The optimum rise time is approximately 3.2 nS.

Note Increase overshoot slightly if the instrument fails the bandwidth test. However, keep the overshoot within the specification.

---

14. Repeat steps 3 through 13 for channel 2.

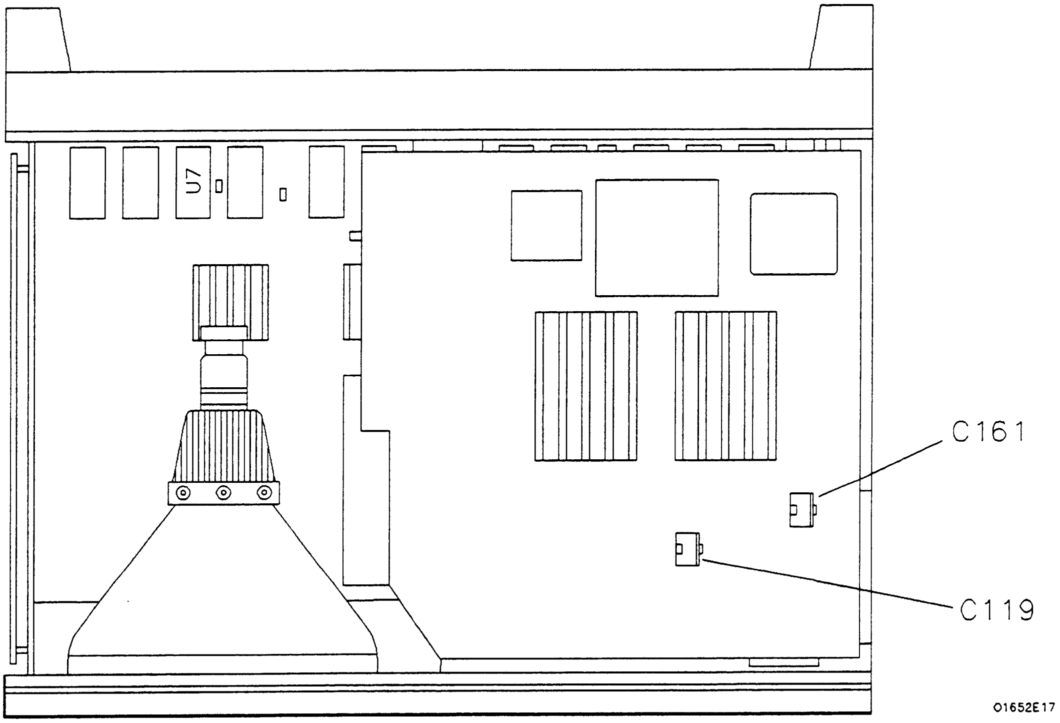


Figure 4-6. High-Frequency Pulse Adjustments

Software Calibration

Software Calibration is accessed through the Trigger menu of the oscilloscope. The calibration procedures in this section should be followed in their entirety and in the same sequence shown.

Note An instrument warm-up of 15 minutes is recommended before starting these procedures.

Offset Calibration

1. In the **System Configuration** menu turn both State/Timing analyzers Off, and turn the oscilloscope On.
2. Press TRACE/TRIG and select **Calibration** using the front-panel knob and SELECT key.

Note

Offset should be listed as the default Calibration choice. If not, select the Calibration choice field and, when the pop-up appears, select **Offset**.

3. Select **Start** with the front-panel knob and SELECT key.

Note

To abort the Offset calibration, select **Cancel** using the front-panel knob and SELECT key.

4. Disconnect all signals from the channel 1 and 2 inputs of the HP 1652B/1653B oscilloscope. Then select **Continue** using the front-panel knob and SELECT key to proceed with the calibration. A message will appear on screen to indicate the instrument is performing the calibration.
5. When the calibration is complete, the updated calibration status appears on screen and the instrument remains in the Calibration menu.

Attenuator Calibration

Equipment Required:

DC Power Supply	HP 6114A
Digital Voltmeter	HP 3478A

6. Select the Calibration choice field and, when the pop-up appears, select **Attenuation.**
7. Connect the power supply to the HP 1652B/1653B oscilloscope and monitor the supply with the digital voltmeter as shown in figure 4-7.

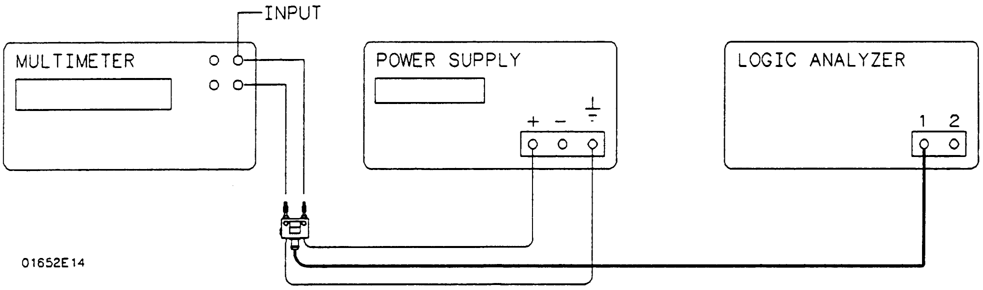


Figure 4-7. Attenuator Calibration Setup

8. Select **Start** with the front-panel knob and SELECT key. The instrument will display the appropriate DC voltages required and prompt you to connect the power supply to the appropriate channel.

Note

To abort the Attenuator calibration, select **Cancel** using the front-panel knob and SELECT key.

9. Adjust the power supply to within 0.1% of the specified voltage. If the measured DC source varies more than 0.1%, select the voltage field with the front-panel knob and SELECT key. Then enter the source level and select DONE.

10. To proceed with the calibration, select **Continue** using the front-panel knob and SELECT key.

11. Repeat steps 9 and 10 for each specified voltage and channel.

12. When the calibration is complete, the updated calibration status appears on screen and the instrument remains in the Calibration menu.

13. Disconnect the power supply from the HP 1652B/1653B inputs.

Gain Calibration

14. Select the Calibration choice field and, when the pop-up appears, select **Gain.**

15. Select **Start** with the front-panel knob and SELECT key.

Note

To abort the Gain calibration, select **Cancel** using the front-panel knob and SELECT key.

---

16. Disconnect all signals from the channel 1 and 2 inputs of the HP 1652B/1653B oscilloscope. Then select **Continue** using the front-panel knob and SELECT key to proceed with the calibration. A message will appear on screen to indicate the instrument is performing the calibration.

17. When the calibration is complete, the updated calibration status appears on screen and the instrument remains in the Calibration menu.

Trigger Calibration

18. Select the Calibration choice field and, when the pop-up appears, select **Trigger level.**

19. Select **Start** with the front-panel knob and SELECT key.

Note

To abort the Trigger calibration, select **Cancel** using the front-panel knob and SELECT key.

---

20. Disconnect all signals from the channel 1 and 2 inputs of the HP 1652B/1653B oscilloscope. Then select **Continue** using the front-panel knob and SELECT key to proceed with the calibration. A message will appear on screen to indicate the instrument is performing the calibration.

21. When the calibration is complete, the updated calibration status appears on screen and the instrument remains in the Calibration menu.

Delay Calibration

22. Select the Calibration choice field and, when the pop-up appears, select **Delay.**

23. Select **Start** with the front-panel knob and SELECT key.

Note

To abort the Delay calibration, select **Cancel** using the front-panel knob and SELECT key.

---

24. Connect a BNC cable from the Probe Compensation output on the rear panel to the channel 1 input of the HP 1652B/1653B oscilloscope. The instrument will prompt you when you need to switch to the channel 2 input.

Note

If you use a 10:1 probe in place of the recommended 1:1 BNC cable, use the BNC-to-mini probe adapter supplied with the instrument. Then set the attenuation field in step 25 to 10:1.

---

25. Set the attenuation field in the calibration menu to the appropriate setting.
26. To proceed with the calibration, select **Continue** using the front-panel knob and SELECT key.
27. When the calibration is complete, the updated calibration status appears on screen and the instrument remains in the Calibration menu.

Caution

Do not execute **Set to Default** after calibrating the instrument. Otherwise, your calibration factors will be replaced by default calibration factors.

---

28. Select **Done** with the front-panel knob and SELECT key to exit the Calibration menu.

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Replaceable Parts

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5

Replaceable Parts

Introduction

This section contains information for ordering parts. Since service support for this instrument is down to the assembly level, the replaceable parts list only includes assemblies and chassis parts. Figure 5-1 shows an exploded view of the HP 1652B/1653B Logic Analyzer.

Abbreviations

Table 5-1 lists the abbreviations used in the parts list and throughout this manual. In some cases two forms of the abbreviations are used: one in all capital letters, and one in partial or no capital letters. However, elsewhere in the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

Replaceable Parts

Table 5-2 is a list of replaceable parts and is organized as follows:

1. Exchange assemblies in alphanumerical order by reference designation.
2. Electrical assemblies in alphanumerical order by reference designation.
3. Chassis-mounted parts in alphanumerical order by reference designation.

The information given for each part consists of the following:

- Reference designation.
- HP part number.
- Part number Check Digit (CD).
- Total quantity (Qty) used in the instrument or on an assembly. The total quantity is given once at the first appearance of the part number in the list.
- Description of the part.
- Typical manufacturer of the part in an identifying five-digit code. All parts in this list (except hardware) are manufactured by or for Hewlett-Packard, code 28480. No list of manufacturers is provided.

Exchange Assemblies

Some parts used in this instrument have been set up for an exchange program. This program allows the customer to exchange a faulty assembly with one that has been repaired, calibrated, and performance-verified by the factory. The cost is significantly less than that of a new part. The exchange parts have a part number in the form XXXXX-695XX.

After receiving the repaired exchange part from Hewlett-Packard, a United States customer has 30 days to return the faulty assembly. For orders not originating in the United States, contact the local HP service organization. If the faulty assembly is not returned within the warranty time limit, the customer will be charged an additional amount. The additional amount will be the difference in price between a new assembly and that of an exchange assembly.

Ordering Information

To order a part in the material list, quote the HP part number, indicate the quantity desired, and address the order to the nearest HP Sales/Service Office.

To order a part not listed in the material list, include the instrument part number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest HP Sales and Service Office.

Direct Mail Order System

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. There are several advantages to this system:

- Direct ordering and shipment from the HP Parts Center in California, USA.
- No maximum or minimum on any mail order (there is a minimum amount for parts ordered through a local HP office when the orders require billing and invoicing).
- Prepaid transportation (there is a small handling charge for each order).
- No invoices.

In order for Hewlett-Packard to provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local HP office. Addresses and telephone numbers are in a separate document included with this manual.

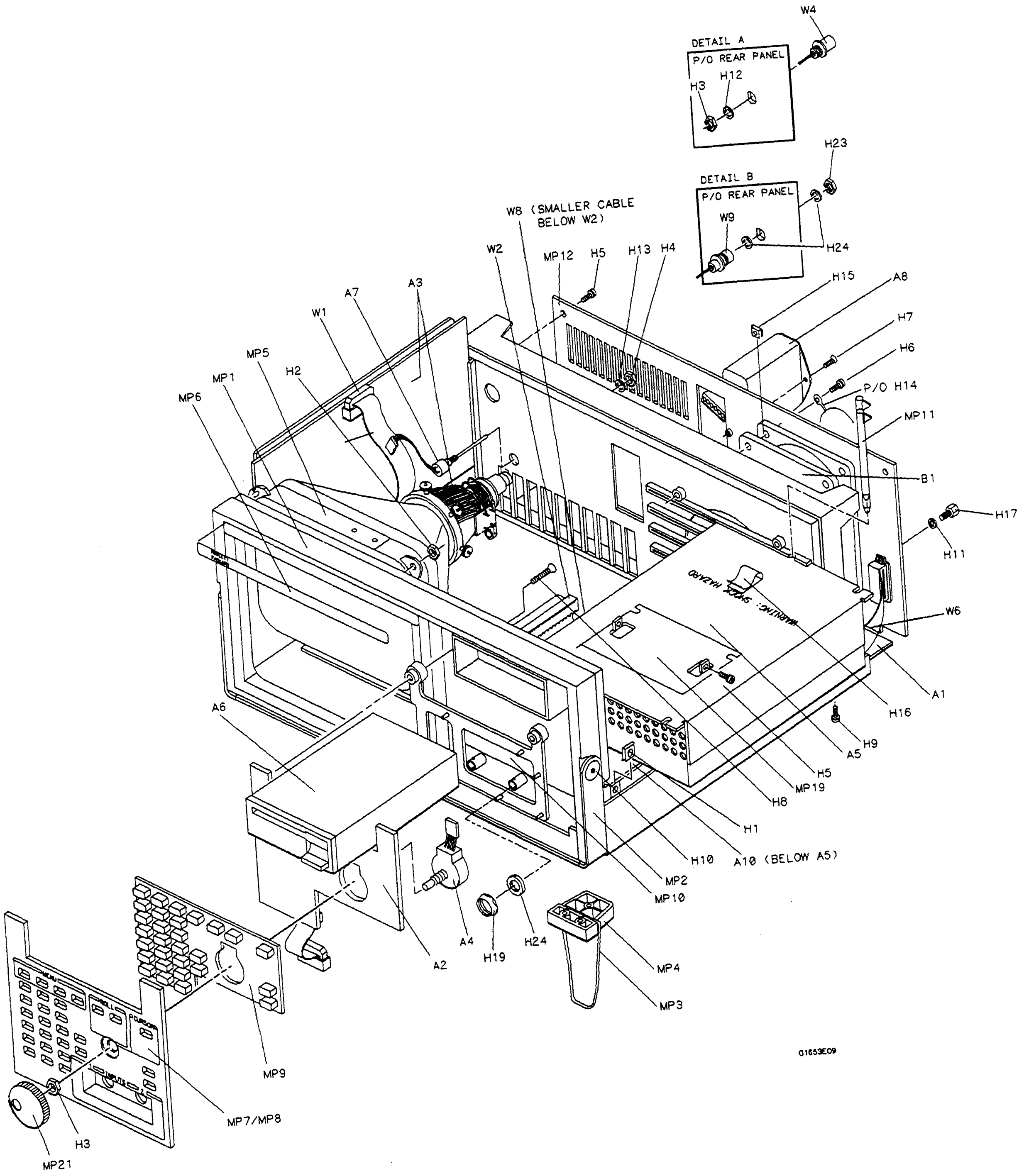
W4
DETAIL A
P/O REAR PANEL
H3
H12
H23
DETAIL B
P/O REAR PANEL
W9
H24
W8 (SMALLER CABLE BELOW W2)
W2
MP12
H5
H13
H4
H15
A8
A7
A3
W1
MP5
MP1
H2
MP6
H7
H6
P/O H14
MP11
B1
H17
H11
WARNING: SHOCK HAZARD
W6
A1
H16
H9
A5
H5
MP19
H8
H1
H10
A10 (BELOW A5)
MP2
MP10
A6
A4
H24
H19
A2
MP4
MP3
MP9
MP7/MP8
H3
MP21
01653E09

Figure 5-1. HP 1652B/1653B Exploded View

Table 5-1. Reference Designator and Abbreviations

REFERENCE DESIGNATOR

A = assembly
B = fan;motor
BT = battery
C = capacitor
CR = diode;diode thyristor; varactor
DL = delay line
DS = annunciator;lamp;LED
E = misc. electrical part
F = fuse
FL = filter
H = hardware
J = electrical connector (stationary portion);jack
L = coil;inductor
MP = misc. mechanical part
P = electrical connector (moveable portion);plug
Q = transistor;SCR; triode thyristor
R = resistor
RT = thermistor
S = switch;jumper
T = transformer
TB = terminal board
TP = test point
U = integrated circuit; microcircuit
V = electron tube; glow lamp
VR = voltage regulator; breakdown diode
W = cable
X = socket
Y = crystal unit(piezo-electric or quartz)

ABBREVIATIONS

A = amperes
A/D = analog-to-digital
AC = alternating current
ADJ = adjust(ment)
AL = aluminum
AMPL = amplifier
ANLG = analog
ANSI = American National Standards Institute
ASSY = assembly
ASTIG = astigmatism
ASYNCHRO = asynchronous
ATTEN = attenuator
AWG = American wire gauge
BAL = balance
BCD = binary-code decimal
BD = board
BFR = buffer
BIN = binary
BRDG = bridge
BSHG = bushing
BW = bandwidth
C = ceramic;cermet (resistor)
CAL = calibrate;calibration
CC = carbon composition
CCW = counterclockwise
CER = ceramic
CFM = cubic feet/minute
CH = choke
CHAM = chamfered
CHAN = channel
CHAR = character
CM = centimeter
CMOS = complementary metal-oxide-semiconductor
CMR = common mode rejection
CNDCT = conductor
CNTR = counter
CON = connector
CONT = contact
CRT = cathode-ray tube
CW = clockwise
D = diameter
D/A = digital-to-analog
DAC = digital-to-analog converter
DARL = darlington
DAT = data
DBL = double
DBM = decibel referenced to 1mW
DC = direct current
DCDR = decoder
DEG = degree
DEMUX = demultiplexer
DET = detector
DIA = diameter
DIP = dual in-line package
DIV = division
DMA = direct memory access
DPDT = double-pole, double-throw
DRC = DAC refresh controller
DRVR = driver

DWL = dowel
ECL = emitter coupled logic
ELAS = elastomeric
EXT = external
F = farads;metal film (resistor)
FC = carbon film/ composition
FD = feed
FEM = female
FF = flip-flop
FL = flat
FM = foam;from
FR = front
FT = gain bandwidth product
FW = full wave
FXD = fixed
GEN = generator
GND = ground(ed)
GP = general purpose
GRAT = graticule
GRV = groove
H = henries;high
HD = hardware
HDND = hardened
HG = mercury
HGT = height
HLCL = helical
HORIZ = horizontal
HP = Hewlett-Packard
HP-IB = Hewlett-Packard Interface Bus
HR = hour(s)
HV = high voltage
HZ = Hertz
I/O = input/output
IC = integrated circuit
ID = inside diameter
IN = inch
INCL = include(s)
INCAND = incandescent
INP = input
INTEN = intensity
INTL = internal
INV = inverter
JFET = junction field-effect transistor
JKT = jacket
K = kilo(103)
L = low
LB = pound
LCH = latch
LCL = local
LED = light-emitting diode
LG = long
LI = lithium
LK = lock
LKWR = lockwasher
LS = low power Schottky
LV = low voltage
M = mega(106);megohms; meter(distance)
MACH = machine
MAX = maximum

MFR = manufacturer
MICPROC = microprocessor
MINTR = miniature
MISC = miscellaneous
MLD = molded
MM = millimeter
MO = metal oxide
MTG = mounting
MTLC = metallic
MUX = multiplexer
MW = milliwatt
N = nano(10-9)
NC = no connection
NMOS = n-channel metal-oxide-semiconductor
NPN = negative-positive-negative
NPRN = neoprene
NRFR = not recommended for field replacement
NSR = not separately replaceable
NUM = numeric
OBD = order by description
OCTL = octal
OD = outside diameter
OP AMP = operational amplifier
OSC = oscillator
P = plastic
P/O = part of
PC = printed circuit
PCB = printed circuit board
PD = power dissipation
PF = picofarads
PI = plug in
PL = plate(d)
PLA = programmable logic array
PLST = plastic
PNP = positive-negative-positive
POLYE = polyester
POS = positive;position
POT = potentiometer
POZI = pozidrive
PP = peak-to-peak
PPM = parts per million
PRCN = precision
PREAMP = preamplifier
PRGMBL = programmable
PRL = parallel
PROG = programmable
PSTN = position
PT = point
PW = potted wirewound
PWR = power
R-S = reset-set
RAM = random-access memory
RECT = rectifier
RET = retainer
RF = radio frequency
RGLTR = regulator
RGTR = register
RK = rack
RMS = root-mean-square

RND = Round
ROM = read-only memory
RPG = rotary pulse generator
RX = receiver
S = Schottky-clamped; seconds(time)
SCR = screw;silicon controlled rectifier
SEC = second(time);secondary
SEG = segment
SEL = selector
SGL = single
SHF = shift
SI = silicon
SIP = single in-line package
SKT = skirt
SL = slide
SLDR = solder
SLT = slot(ted)
SOLD = solenoid
SPCL = special
SQ = square
SREG = shift register
SRQ = service request
STAT = static
STD = standard
SYNCHRO = synchronous
TA = tantalum
TBAX = tubeaxial
TC = temperature coefficient
TD = time delay
THD = thread(ed)
THK = thick
THRU = through
TP = test point
TPG = tapping
TPL = triple
TRANS = transformer
TRIG = trigger(ed)
TRMR = trimmmer
TRN = turn(s)
TTL = transistor-transistor
TX = transmitter
U = micro(10-6)
UL = Underwriters Laboratory
UNREG = unregulated
VA = voltampere
VAC = volt,ac
VAR = variable
VCO = voltage-controlled oscillator
VDC = volt,dc
VERT = vertical
VF = voltage,filtered
VS = versus
W = watts
W/ = with
W/O = without
WW = wirewound
XSTR = transistor
ZNR = zener
oC = degree Celsius (Centigrade)
oF = degree Fahrenheit
oK = degree Kelvin

Table 5-2. Replaceable Parts List

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	01652-66501	0	1	SYSTEM BOARD ASSEMBLY – 80 CHANNEL (1652B)	28480	01652-66501
A1	01653-66501	1	1	SYSTEM BOARD ASSEMBLY – 32 CHANNEL (1653B)	28480	01653-66501
A2	01652-66503	2	1	KEYBOARD CIRCUIT BOARD ASSEMBLY	28480	01652-66503
A3	2090-0204	9	1	MONITOR ASSEMBLY	28480	2090-0204
A4	0960-0753	6	1	ROTARY PULSE GENERATOR	28480	0960-0753
A5	0950-1879	8	1	POWER SUPPLY ASSEMBLY	28480	0950-1879
A6	0950-1798	0	1	DISK DRIVE ASSEMBLY	28480	0950-1798
A7	01650-61614	4	1	INTENSITY ADJUSTMENT ASSEMBLY	28480	01650-61614
A8	9135-0325	8	1	LINE FILTER SWITCH ASSEMBLY	28480	9135-0325
A9	01650-61608	6	5	PROBE TIP ASSEMBLY (1652B)	28480	01650-61608
A9	01650-61608	6	2	PROBE TIP ASSEMBLY (1653B)	28480	01650-61608
A10	01652-66502	1	1	OSCILLOSCOPE BOARD ASSEMBLY - 2 CHANNEL	28480	01652-66502
A11	54503-63401	4	2	ATTENUATOR ASSEMBLY	28480	54503-63401
A12	10430A	8	2	PROBE 500 MHZ 1M 10:1	28480	10430A
B1	3160-0429	0	1	FAN-TUBEAXIAL 100-CFM 12VDC	28480	3160-0429
E1	5959-9333	8	0	REPLACEMENT PROBE LEADS (PKG OF 5)	28480	5959-9333
E2	5959-9334	9	0	REPLACEMENT PROBE GROUNDS (PGK OF 5)	28480	5959-9334
E3	5959-9335	0	0	REPLACEMENT POD GROUNDS (PKG OF 5)	28480	5959-9335
E4	5959-0288	4	5	GRABBER ASSEMBLY SET – 20 (1652B)	28480	5959-0288
E4	5959-0288	4	2	GRABBER ASSEMBLY SET-20 (1653B)	28480	5959-0288
F1	2110-0003	0	1	FUSE 3A 250V NTD FE UL	28480	2110-0003
H1	0535-0113	1	10	NUT "U"-TP M3 X 0.500.3MM-THK (TOP COVER)	28480	0535-0113
H2	0535-0056	1	4	NUT-HEX PRVLG-TRQ M4 X 0.7 5MM-THK (CRT)	28480	0535-0056
H3	2950-0001	8	3	NUT-DBL-CHAM 3/8-32-THD0.094-IN-THK (RPG, BNC)	28480	2950-0001
H4	2950-0072	3	1	NUT-DBL-CHAM 1/4-32-THD0.062-IN-THK (INTEN ADJ)	28480	2950-0072
H5	0515-0372	2	12	SCREW M3 X 0.5 8MM-LG (DISK DRIVE, REAR PANEL)	28480	0515-0372
H6	0515-0821	6	4	SCREW- M3.5 X 0.6 (FAN)	28480	0515-0821
H7	0515-1035	6	22	SCREW-M3 X 0.5 8MM- (FEET, LINE FIL, TOP COVER)	28480	0515-1035
H8	0515-1135	7	4	SCREW- M3 X 0.5 25MM-LG (KEYPAD)	28480	0515-1135
H9	0515-1951	5	8	SCREW-TAPPING M4.2 (SYSTEM BOARD)	28480	0515-1951
H10	01650-82401	1	2	M5 SHOULDER SCREW (HANDLE)	28480	01650-82401
H11	2190-0009	4	2	WASHER-LK INTL T NO. 80.168-IN-ID (HP-IB CABLE)	28480	2190-0009
H12	2190-0016	3	2	WASHER-LK INTL T 3/8 IN0.377-IN-ID (BNC)	28480	2190-0016
H13	2190-0027	6	1	WASHER-LK INTL T 1/4 IN0.256-IN-ID (INTEN ADJ)	28480	2190-0027
H14	3160-0092	3	1	FAN GUARD	28480	3160-0092
H15	0590-1868	1	4	FAN MOUNTING CLIP	28480	0590-1868
H16	1400-0611	0	1	CLAMP-FL-CA 1-WD (DISK DRIVE CABLE)	28480	1400-0611
H17	0380-1482	5	2	HEX STANDOFF .0340 (HP-IB CABLE)	28480	0380-1482
H18	01650-00203	3	2	NUT PLATE (HANDLE)	28480	01650-00203
H19	2950-0054	1	2	NUT 1/2 - 28 .125 (ATTENUATOR BNC)	28480	2950-0054
H20	3050-0893	9	2	WASHER - FLAT (PC BOARD BRACKET)	28480	3050-0893

Table 5-2. Replaceable Parts List (continued)

Reference Designator	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
H21	0515-0374	4	6	SCREW-MACH M3.0 X 0.50 (OSCILLOSCOPE BOARD)	28480	0515-0374
H22	0515-1246	1	4	SCREW-MACH M3 X 0.5 (ATTENUATOR)	28480	0515-1246
H23	2950-0035	8	1	NUT .468-32 .078 (PROBE COMPENSATION BNC)	28480	2950-0035
H24	2190-0068	5	3	WASHER-LK .505 .630 .02 (ATTENUATOR)	28480	2190-0068
MP1	01650-45207	7	1	CABINET MOLDED PLASTIC	28480	01650-45207
MP2	01650-04901	2	1	BALE HANDLE	28480	01650-04901
MP3	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP4	01650-47701	0	2	MOLDED FOOT	28480	01650-47701
MP5	01650-01202	0	1	GROUND BRACKET	28480	01650-01202
MP6	01652-94302	8	1	IDENTIFICATION LABEL (1652B)	28480	01652-94302
MP6	01653-94302	9	1	IDENTIFICATION LABEL (1653B)	28480	01653-94302
MP7	01652-94301	7	1	KEYBOARD LABEL	28480	01652-94301
MP8	01652-40501	6	1	KEYBOARD HOUSING	28480	01652-40501
MP9	01652-41901	2	1	ELASTOMERIC KEYPAD	28480	01652-41901
MP10	01652-40502	7	1	KEYBOARD SPACER	28480	01652-40502
MP11	01650-46101	2	2	LOCKING PIN PCB	28480	01650-46101
MP12	01650-00205	1	1	REAR PANEL (1652B)	28480	01650-00205
MP12	01651-00203	0	1	REAR PANEL (1653B)	28480	01651-00203
MP13	7120-4835	0	1	CSA CERTIFICATION LABEL	28480	7120-4835
MP14	01650-04101	4	1	TOP COVER	28480	01650-04101
MP15	01650-84501	6	1	ACCESSORY POUCH	28480	01650-84501
MP16	01650-94303	7	1	PROBE LABELS	28480	01650-94303
MP17	01650-29101	6	5	GROUND SPRING (SYSTEM BOARD 1652B)	28480	01650-29101
MP17	01650-29101	6	2	GROUND SPRING (SYSTEM BOARD 1653B)	28480	01650-29101
MP18	01650-29102	7	1	CLIP RS-232 ESD	28480	01650-29102
MP19	01650-25401	1	1	DISK INSULATOR	28480	01650-25401
MP20	01650-63202	0	1	RS-232 LOOPBACK CONNECTOR	28480	01650-63202
MP21	01650-47401	7	1	RPG KNOB	28480	01650-47401
MP22	01652-01201	1	1	BRACKET - PC BD (OSCILLOSCOPE BOARD)	28480	01652-01201
MP23	01652-01202	2	1	PLATE - PC BD (OSCILLOSCOPE BOARD)	28480	01652-01202
MP24	01652-94303	9	1	PROBE COMPENSATION LABEL	28480	01652-94303
W1	01650-61601	9	1	SWEEP CABLE	28480	01650-61601
W2	54503-61606	7	1	POWER SUPPLY CABLE	28480	54503-61606
W3	01650-61604	2	1	DISK CABLE	28480	01650-61604
W4	01650-61605	3	2	BNC CABLE	28480	01650-61605
W5	01650-61607	5	5	PROBE CABLE (1652B)	28480	01650-61607
W5	01650-61607	5	2	PROBE CABLE (1653B)	28480	01650-61607
W6	01650-61613	3	1	HP-IB CABLE	28480	01650-61613
W7	01650-61616	6	1	FAN CABLE	28480	01650-61616
W8	01652-61602	2	1	OSCILLOSCOPE CABLE ASSY 60 COND	28480	01652-61602
W9	54100-61610	6	1	PROBE COMPENSATION BNC	28480	54100-61610

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6A

Theory of Operation

Introduction

This section provides the theory of operation of the HP 1652B/1653B Logic Analyzer. The theory of operation is included for information only and is not intended for troubleshooting purposes.

Safety

Read the Safety Summary at the front of this manual before servicing the instrument. Before performing any procedure, review it for cautions and warnings.

Warning

Maintenance should be performed by trained service personnel aware of the hazards involved (for example, fire and electric shock). When maintenance can be performed without power applied, the power cord should be removed from the instrument.

Block Level Theory

The HP 1652B is an 80 channel state and timing logic analyzer with a 2 channel, 100 MHz, 400 Msample/s digitizing oscilloscope. The HP 1653B is a 32 channel state and timing logic analyzer with a 2 channel, 100 MHz, 400 Msample/s digitizing oscilloscope. The human interface is a front-panel keypad and knob for instrument control and a 9-inch (diagonal) white phosphor CRT for information display. Available on the rear panel are RS-232-C and HP-IB ports for communication to a printer or from a controller. Also on the rear panel are two BNCs for input or output of an external trigger and a BNC for oscilloscope probe compensation.

The instrument is built around the 68000 microprocessor and powerful data acquisition ICs that probe, shape, store, and analyze data from a target system. An acquisition interface to the 68000 makes the data acquisition system fully compatible with the architecture of the 68000 microprocessor. The System Assembly Board contains the necessary circuitry to interface the keypad, CRT monitor, disk drive, RS-232-C, and HP-IB ports.

Figures 6A-1 and 6A-2 show a simplified block diagram of the instrument.

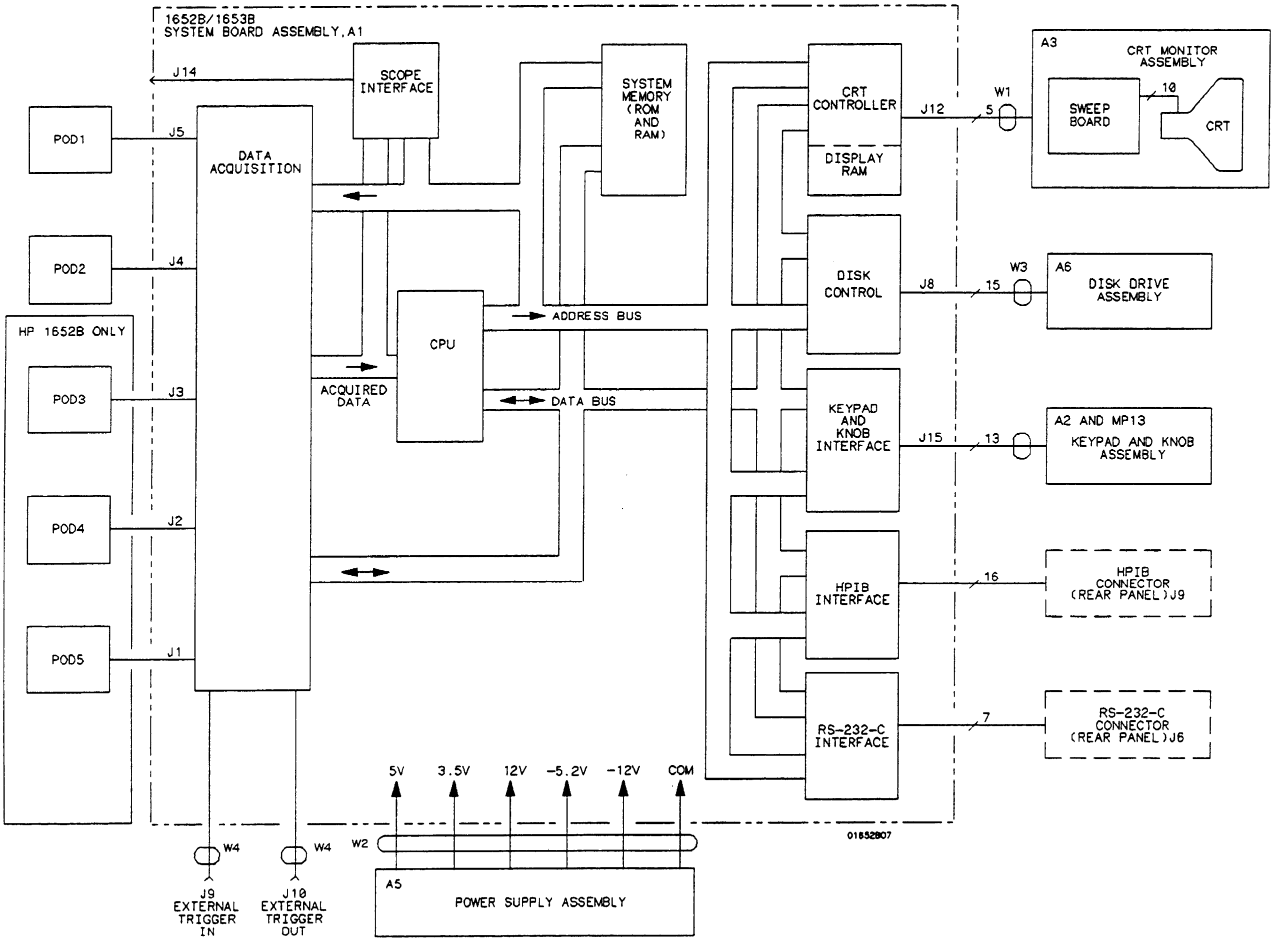
1652B/1653B SYSTEM BOARD ASSEMBLY, A1
J14
SCOPE INTERFACE
SYSTEM MEMORY (ROM AND RAM)
CRT CONTROLLER
DISPLAY RAM
J12
W1
5
A3
CRT MONITOR ASSEMBLY
SWEEP BOARD
10
CRT
POD1
J5
DATA ACQUISITION
POD2
J4
DISK CONTROL
J8
W3
15
A6
DISK DRIVE ASSEMBLY
HP 1652B ONLY
CPU
ADDRESS BUS
POD3
J3
ACQUIRED DATA
DATA BUS
KEYPAD AND KNOB INTERFACE
J15
13
A2 AND MP13
KEYPAD AND KNOB ASSEMBLY
POD4
J2
HPIB INTERFACE
16
HPIB CONNECTOR (REAR PANEL) J9
POD5
J1
RS-232-C INTERFACE
7
RS-232-C CONNECTOR (REAR PANEL) J6
5V
3.5V
12V
-5.2V
-12V
COM
01652B07
W4
W4
W2
J9 EXTERNAL TRIGGER IN
J10 EXTERNAL TRIGGER OUT
A5
POWER SUPPLY ASSEMBLY

Figure 6A-1. System Board Assembly Block Diagram

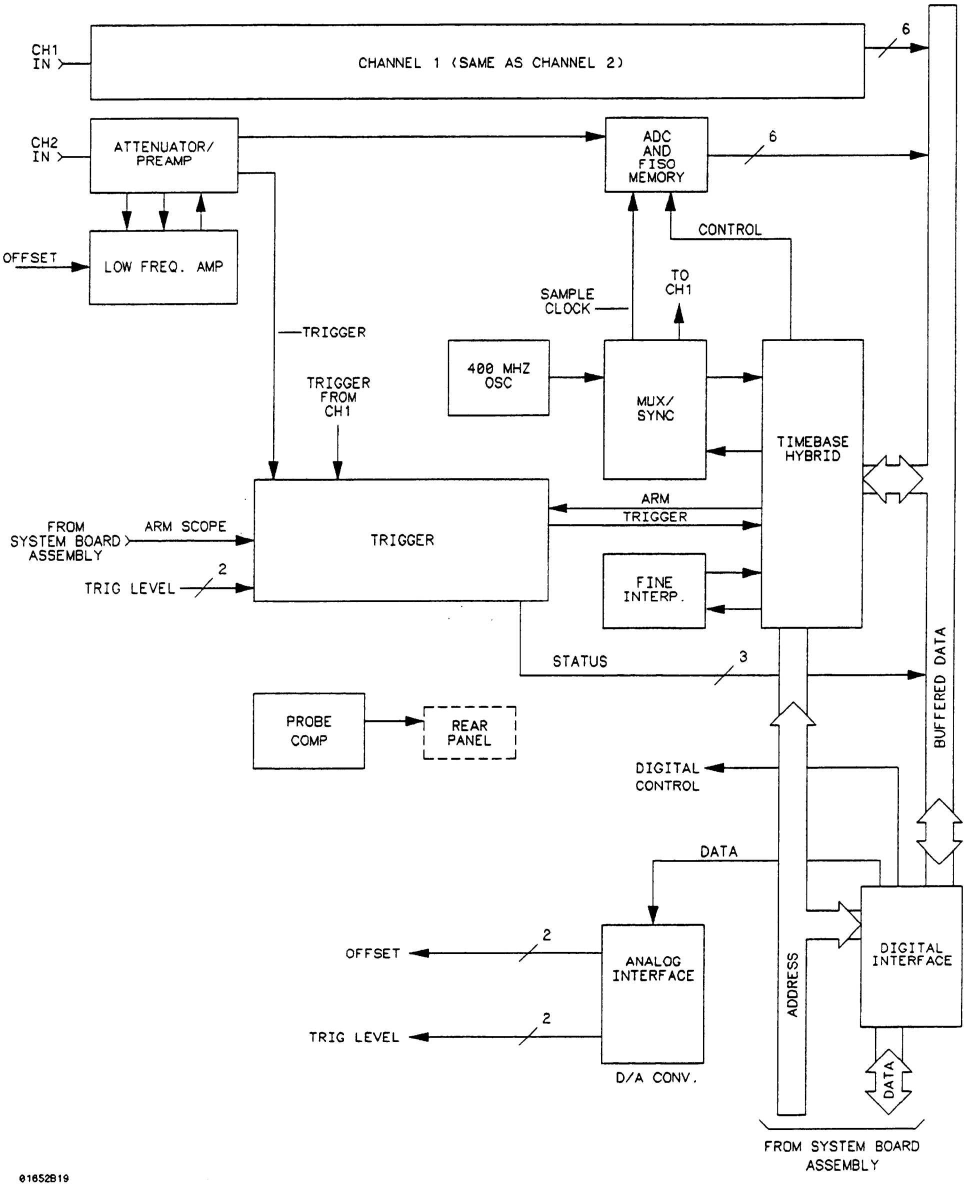
CH1 IN
CHANNEL 1 (SAME AS CHANNEL 2)
6
CH2 IN
ATTENUATOR/ PREAMP
ADC AND FISO MEMORY
6
OFFSET
LOW FREQ. AMP
CONTROL
SAMPLE CLOCK
TO CH1
TRIGGER
400 MHZ OSC
MUX/ SYNC
TRIGGER FROM CH1
TIMEBASE HYBRID
ARM
TRIGGER
FROM SYSTEM BOARD ASSEMBLY
ARM SCOPE
TRIGGER
2
TRIG LEVEL
FINE INTERP.
STATUS
3
BUFFERED DATA
PROBE COMP
REAR PANEL
DIGITAL CONTROL
DATA
2
OFFSET
ANALOG INTERFACE
2
TRIG LEVEL
D/A CONV.
ADDRESS
DIGITAL INTERFACE
DATA
FROM SYSTEM BOARD ASSEMBLY
01652B19

Figure 6A-2. Oscilloscope Assembly Block Diagram

Power Supply Assembly

The switching power supply provides 120 W (200 W maximum) for the instrument. The ac input to the power supply is 115V or 230 V, -25% to +15%. Maximum input power is 350 VA maximum. The ac input frequency is 48 to 66 Hz.

All voltages necessary to operate the instrument are applied first to the Main Assembly. Unfiltered voltages of + 15V, +12V, -12V, +5.15V, -5.2V, and +3.5V are supplied to the board where they are then filtered and distributed throughout the main assembly board, oscilloscope board, and to the CRT Monitor Assembly. Filtered voltages of approximately +5 V and +12 V are routed through the Main Assembly to the CRT Monitor Assembly. The +5.15 V supply is adjustable on the supply.

CRT Monitor Assembly

The CRT Monitor Assembly consists of the sweep board circuitry, a 9-inch white phosphor CRT, and the CRT yoke. The assembly requires + 5 V and +12 V from the power supply via the Main Assembly.

The non-interlacing raster display is controlled by the CPU portion of the Main Assembly. System control provides synchronization and pixel information.

Main Assembly

The Main Assembly contains the logic analyzer acquisition system and system control circuitry. It also provides interfaces for the Power Supply Assembly, CRT Monitor Assembly, keyboard, RS-232C, and HP-IB. The input to the Main Assembly is from any or all of the data acquisition pods, which exit the rear panel. The user interface is from the front-panel keyboard or with a controller via the HP-IB or RS-232C connector on the rear panel. A more detailed theory of the logic analyzer circuitry follows block level theory.

Central Processing Unit (CPU)

The CPU is a 68000 P10 microprocessor with addressing capability of 16 megabytes (23 address lines/16 data lines). The CPU receives its clock (10 MHz) from the TCL (Timing Control Logic). The TCL circuitry consists of programmable array logic (PALs), various logic gates, and miscellaneous circuitry for arbitrating between display and refresh requests of display and system RAM. The PALs and arbitration circuitry are synchronized with a 20 MHz clock. The rest of the circuitry is asynchronous. The signals generated by the TCL provide all timing for the CPU. The CPU drives the read/write line and the address and data strobes.

The CPU supplies a 2.5 MHz enable clock for synchronization with the CRT Controller (CRTC).

Oscilloscope Assembly

The Oscilloscope Assembly contains the oscilloscope acquisition system. The analog input to the Oscilloscope Assembly is from either or both of two channels, located at the front-panel BNCs. The user interface is from the front-panel keyboard or with a controller via the HP-IB or RS-232C connector on the rear panel. A more detailed theory of the Oscilloscope Assembly follows the block level theory.

Keypad and Knob Assembly

The front-panel keypad is elastomeric and has 29 keys. The keyboard rows are continually scanned at a frequency of 60 Hz. When a key is pressed the signal is sent as data to the 68000 which determines the key pressed and its function. The Rotary Pulse Generator (RPG) is connected to the front-panel knob and supplies pulses to the 68000 microprocessor when the knob is turned. The RPG is used for cursor movement and value entry.

Disk Controller

The disk controller performs the necessary functions for reading or writing data to the built-in disk drive of the logic analyzer. The disk controller interface to the 68000 is an 8-bit bidirectional bus for data, status, and control word transfers.

The built-in disk drive is a 3.5-inch double-sided Sony disk drive. The main features of the disk drive are low power consumption, low height, and high reliability with simple mechanism and electronic circuitry.

RS-232-C Interface

The controlling IC of the RS-232-C Interface is a Signetics SCN2661 Enhanced Programmable Communications Interface (EPCI) which is a universal synchronous/asynchronous receiver/transmitter (USART) data communications IC.

The SCN2661 serializes parallel data from the 68000 for transmission. At the same time, it also receives serial data and converts it to parallel data characters for the 68000.

The SCN2661 IC contains a baud rate generator which can be programmed from the logic analyzer I/O menu for one of eight baud rates. Protocol, word length, stop bits length, and parity are also programmed via the I/O menu.

Two additional ICs, the DS14C88 and DS14C89, are line drivers/receivers used by the SCN2661 IC for interface of terminal equipment with data communications equipment. Slew rate control is provided on the ICs, eliminating the need for external capacitors.

HP-IB Interface

The HP-IB controller provides an interface between the microprocessor system and the HP-IB in accordance with IEEE 488 standards. An 8-bit data buffer and 8-bit control line buffer interface the HP-IB controller to the HP-IB bus.

The HP-IB is a 24 conductor shielded cable carrying 8 data lines, 8 control lines, 7 system grounds, and 1 chassis ground.

Logic Analyzer Theory of Operation

The HP 1652B/1653B logic analyzer operation is based around a 68000 microprocessor and proprietary acquisition ICs. Input data is captured by passive probing, reshaped, and stored into memory.

Data Acquisition

The data acquisition for the logic analyzer consists of the data acquisition pods, acquisition ICs, and the interface to the 68000. The interface to the target system is through any of the data acquisition pods. There are five pods available on the HP 1652B (80 channels) and two pods available on the HP 1653B (32 channels). Each pod contains 16 input data probes and one external clock input for state mode measurements. The data probes can be used for state or timing measurements.

Each pod consists of a probe tip assembly and a 4.5 foot woven cable. A probe tip assembly includes 17 twelve-inch probes and a common ground return. This is connected to one end of the cable. The other end of the woven cable terminates at the rear panel of the logic analyzer. The woven cable consists of 17 signal lines, 17 signal return lines, 2 chassis grounds, and 2 power supply lines. All are woven together with polyarmid yarn.

Each probe input has an input impedance of 100k ohms in parallel with approximately 8 pF. The probes can be grounded in two ways: with a common pod ground for state measurements, or with a probe tip ground for higher frequency measurements.

The input signals are attenuated by a factor of 10 in the passive probe. The signals are applied to a comparator where they are compared against a voltage threshold to determine if the voltage level is above or below the threshold level. The comparator then shapes the single-ended signal and outputs it at an ECL level to the acquisition IC. The input data is then stored at the acquisition IC.

Arming Control

The two BNCs on the rear panel are used for arming control of the logic analyzer acquisition ICs. An arm signal may be output from the ICs to the rear panel EXTERNAL TRIGGER OUT (J10), or input to the ICs from EXTERNAL TRIGGER IN (J9).

Memory

The memory of the logic analyzer consists of three separate memories: one ROM and two RAMs. The system (EP)ROM is 32 K long by 16 wide and is used primarily for booting-up the system and self-test storage. The system (D)RAM is 512 K long by 16 wide and contains the operating system and the acquired data from the target system. Since the RAM is a volatile memory, the operating system is loaded at each power-up of the instrument via the built-in disk drive and a mini floppy disk.

The display (D)RAM is 64K long by 4 wide and is cycle shared between the 68000 and the display refresh circuitry. This is why the display bus is separate from the local bus. The two buses are separated by a set of address multiplexers and data buffers.

Oscilloscope Theory of Operation

The oscilloscope circuitry provides the conditioning, sampling, digitizing, and storage of the signals at the channel input connectors. The channels are identical. The trigger circuitry input can be selected between the oscilloscope channels and the logic analyzer. A 400 MHz oscillator, with the time base and mux/sync (multiplexer synchronizer), provides the sample clocking. After conditioning, the signals are digitized and stored in a hybrid IC containing both the ADC and memory. The signal data is then transferred over the data bus where it is processed for display.

Attenuator/ Preamps

The channel signals are conditioned by the attenuator/preamps, thick film hybrids containing passive attenuators, impedance converters, and a programmable amplifier. The channel sensitivity defaults to the standard 1-2-5 sequence (other sensitivities can be set also). However, the firmware uses passive attenuation of 1, 5, 25, and 125, with the programmable preamp, to cover the entire sensitivity range.

The input has a selectable 1 MΩ or 50 Ω input impedance. Compensation for the passive attenuators is laser trimmed and not adjustable. After the passive attenuators, the signal is split into high-frequency and low-frequency components. Low frequency components are amplified on the PC board where they are combined with the offset voltage.

The high- and low-frequency components of the signal are recombined and applied to the input FET of the preamp. The FET provides a high input impedance for the preamp. The programmable preamp adjusts the gain to suit the required sensitivity and provides two output signals. One signal is the same polarity as the input and goes to the trigger circuitry. The other is of the opposite polarity and is sent to the post amplifier.

Post Amplifier

The post amplifier conditions the signal for the ADC. It has a gain of approximately 2.5 and it has one compensation capacitor adjustment per channel. This adjustment effects the transition rise time and overshoot.

ADC and FISO Memory

A single hybrid digitizes and stores the channel signal. Digitization is done by a set of comparators in a flash converter. A precision voltage divider within the ADC provides a separate reference for each comparator. This voltage divider is controlled by a reference supply and amplifier on the PC board.

The FISO (fast in, slow out) memory is 2 k by 6-bit bytes. Sample clocks are provided by the time base circuitry. At 500 ns/div and faster, the sample clock is 400 MHz. At sweep speeds of 1 us and slower, the sample clocks range from 200 MHz to 25 Hz. The FISO data is buffered onto the CPU data bus for further processing.

Triggering

The trigger circuitry accepts inputs from both oscilloscope channels, the logic analyzer, and the time base. Only one of these signals is multiplexed into the trigger circuitry, depending on the trigger mode. For example, the input from the time base is used while the instrument is in the "trigger immediate" mode.

When in the "edge trigger" mode, the preamp outputs are fed through a high speed voltage comparator using a reference voltage from the DAC.

The trigger circuitry output drives the time base and the logic analyzer arming input. This output and internal status signals are interfaced to the data bus for software processing purposes.

Time Base

The time base provides the sample clocks and timing necessary for data acquisition. It consists of the 400 MHz reference oscillator, mux/sync hybrid (multiplexer/synchronizer), and time base IC.

The mux/sync hybrid provides sample clocks to the ADC. At sample rates of 400 MHz and 200 MHz, this sample clock is derived from the 400 MHz reference oscillator. At 100 MHz and slower, the sample clock comes from the time base IC. The mux/sync hybrid synchronizes the gating of the sample clock to provide only full sample clocks.

The time base hybrid has programmable dividers to provide the rest of the sample frequencies appropriate for the time range selected. It uses the time-stretched output of the fine interpolator to time-reference the sampling to the trigger point. It has counters to control how much data is taken before (pre-trigger data) and after (post-trigger data) the trigger event. After the desired number of pre-trigger samples has occurred, the time base hybrid sends a signal to the Logic Trigger (trigger arm) indicating it is ready for the trigger event. When the trigger condition is satisfied, the Logic Trigger sends a signal back to the time base hybrid. The time base hybrid then starts the post-trigger delay counter. When the countdown reaches zero, the sample clocks are stopped and the CPU is signaled that the acquisition is complete.

Fine Interpolator

The Fine Interpolator is a dual-slope integrator that acts as a time-interval stretcher. When the trigger circuitry receives a signal that meets the programmed triggering requirements, it signals the time base. The time base then sends a pulse to the fine interpolator. The pulse is equal in width to the time between the trigger and the next sample clock. The fine interpolator stretches this time by a factor of approximately 375. Meanwhile, the time base hybrid runs a counter with a clock derived from the sample rate oscillator. When the interpolator indicates the stretch is complete, the counter is stopped. The count represents, with much higher accuracy, the time between the trigger and the first sample clock. The count is stored and used to place the recently acquired data in relationship with previous data.

Probe Compensation

An oscillator generates a 1.25 kHz square wave with fast edges for oscilloscope probe compensation. The oscillator's levels range from approximately -400 mV to -900 mV.

Digital Interface

The Digital Interface provides control and interface between the system control and digital functions in the acquisition circuitry.

Analog Interface

The Analog Interface provides control of analog functions in the acquisition circuitry. It is primarily a 16 channel DAC with an accurate reference, and filters on the outputs. It controls channel offsets and trigger levels.

Contents

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Self Tests

Introduction

This section provides information on the power-up self tests and extended self tests of the HP 1652B/1653B. All of these self tests may be performed without access to the interior of the instrument.

Power-Up Self Tests

The power-up self tests are automatically performed upon applying power to the instrument. The revision number of the operating system is given in the upper right corner of the screen during the power-up self tests. As each test is completed, either "passed" or "failed" is printed in front of the name of each test in the following manner:

```
PERFORMING POWER-UP SELF-TESTS

  passed  ROM test
  passed  RAM test
  passed  Interrupt test
  passed  Display test
  passed  Keyboard test
  passed  Acquisition test
  passed  Threshold test
  passed  Disk test

LOADING SYSTEM FILE
```

As indicated by the last message, the HP 1652B/1653B logic analyzer will automatically load from the operating system disk in the disk drive. If the operating system disk is not in the disk drive, the message "SYSTEM DISK NOT FOUND" will be displayed at the bottom of the screen and "NO DISK" will be displayed in front of the disk test in place of "passed."

Note

If the message "SYSTEM DISK NOT FOUND" appears on screen, insert the operating system disk into the disk drive and press any front panel key.

Selectable Self Tests

Selectable self tests are used as troubleshooting aids. Eight self tests may be invoked via the Self Tests menu:

- Analyzer Data Acquisition
- Scope Data Acquisition
- RS-232-C
- BNC
- Keyboard
- RAM
- ROM
- Disk Drive
- Cycle through tests

The required test is selected by moving the cursor to the test and pressing the front panel SELECT key. A pop-up menu will appear with a description of the test to be performed. The self test does not begin until the cursor is placed on Single test, Repetitive test, or Execute and the front panel SELECT key is pressed.

The repetitive self tests display the number of "runs" and "failures" for the selected test. Press STOP to discontinue the test.

After the test is completed, either "Passed,""Failed," or "Tested" will be displayed on the Self Tests menu in front of the test.

Selecting the Self Tests Menu

The self tests may be invoked from any menu by pressing the front panel I/O key. The pop-up I/O menu appears on screen with the following choices:

- Done
- Print Screen
- Print All
- Disk Operations
- I/O Port Configuration
- External BNC Configuration
- Self Tests

1. Move the cursor to **Self Tests** with the front panel knob and press SELECT.

Caution ✋

The self tests are loaded from the Performance Verification disk. The process of running the self tests destroys the current configuration and data.

2. Insert the Performance Verification disk (or copy of it) into the disk drive.

3. Move the cursor to the **Start self test** field with the front panel knob and press SELECT. After loading the self tests, the HP 1652B/1653B Self Tests menu will display the following:

Untested * Analyzer Data Acquisition
Untested * Scope Data Acquisition
Untested * RS-232-C
Untested * BNC
Untested * Keyboard
Untested * RAM
Untested * ROM
Untested * Disk Drive
*** Cycle through tests**

4. To select a self test, move the cursor to the appropriate test with the front panel knob and press SELECT. To leave the HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT. The HP 1652B/1653B will reload the operating system from the disk and display the default System Configuration menu.

Note

The operating system disk (or copy of it) must be in disk drive to reload the operating system after leaving the Self Tests menu.

Analyzer Data Acquisition Self Test

The Analyzer Data Acquisition self test verifies the functionality of key elements of the internal acquisition system.

1. In HP 1652B/1653B Self Tests menu, move the cursor to **Analyzer Data Acquisition** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.

2. Move the cursor to **Single test** or **Repetitive test** and press SELECT. The message "Running Data Acquisition Test" appears on screen while the instrument is performing the test. When the test is finished, the message "Data Acquisition Test complete" will appear on screen.

3. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.

4. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

Scope Data Acquisition Self Test

The Scope Data Acquisition self test verifies the functionality of key elements of the internal acquisition system. These key elements include the following:

- Scope Memory
- Scope Pretrigger Delay
- Scope Trigger
- Scope Sample Rate
- Scope Preamp
- Scope Interpolator

1. In HP 1652B/1653B Self Tests menu, move the cursor to **Scope Data Acquisition** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.

2. Move the cursor to **Single test** or **Repetitive test** and press SELECT. The message "Running Scope Data Acquisition Test" appears on screen while the instrument is performing the test. When the test is finished, the message "Scope Data Acquisition Test complete" will appear on screen.

3. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.

4. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

RS-232-C Self Test

The RS-232-C self test verifies the functionality of the RS-232-C driver and continuity of the RS-232-C data paths.

Equipment Required:

RS-232-C Loopback Connector 01650-63202

Procedure:

1. In HP 1652B/1653B Self Tests menu, move the cursor to **RS-232-C** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.

2. Connect the RS-232-C loopback connector to the rear-panel RS-232-C receptacle. The message "Running RS-232C Test" appears on screen while the instrument is performing the test. When the test is finished, the message "RS-232C Test complete" will appear on screen.

Note The RS-232-C loopback connector is an accessory supplied with the HP 1652B/1653B.

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3. Move the cursor to **Single test** or **Repetitive test** and press SELECT.

4. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.

5. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

BNC Self Test

The BNC self test verifies the functionality of the internal BNC trigger circuitry.

1. In HP 1652B/1653B Self Tests menu, move the cursor to **BNC** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.
2. Move the cursor to **Single test** or **Repetitive test** and press SELECT.The message "Running BNC Test" appears on screen while the instrument is performing the test. When the test is finished, the message "BNC Test complete" will appear on screen.
3. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.
4. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

Keyboard Self Test

The Keyboard self test verifies the key closures and knob operation on the front panel system.

1. In HP 1652B/1653B Self Tests menu, move the cursor to **Keyboard** and press SELECT. A menu will appear with a description of the test and fields to Execute the test or exit the menu (Done).
2. Move the cursor to **Execute** and press SELECT. A menu displaying the front-panel keys will appear on screen.
3. Press all of the keys on the front panel keypad and rotate the front panel RPG knob to verify their operation.
4. Press the front-panel STOP key twice to return to the Keyboard Self Test menu.
5. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

RAM Self Test

The RAM self test verifies the operation of system RAM and display RAM.

1. In HP 1652B/1653B Self Tests menu, move the cursor to **RAM** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.
2. Move the cursor to **Single test** or **Repetitive test** and press SELECT.The message "Running RAM Test" appears on screen while the instrument is performing the test. When the test is finished, the message "RAM Test complete" will appear on screen.
3. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.

4. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

ROM Self Test

The ROM self test verifies the operation of system ROM.

1. In HP 1652B/1653B Self Tests menu, move the cursor to **ROM** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.
2. Move the cursor to **Single test** or **Repetitive test** and press SELECT.The message "Running ROM Test" appears on screen while the instrument is performing the test. When the test is finished, the message "ROM Test complete" will appear on screen.
3. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.
4. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

Disk Drive Self Test

The Disk Drive self test verifies the functionality of the key elements of the internal disk drive system.

1. In HP 1652B/1653B Self Tests menu, move the cursor to **Disk Drive** and press SELECT. A menu will appear with a description of the test, the number of "runs" and "failures" for the selected test, and fields to select Single test, Repetitive test, or Done.

Note

There must be a formatted disk in the disk drive to successfully run the Disk Drive self tests.

---

2. Move the cursor to **Single test** or **Repetitive test** and press SELECT.The message "Running Disk Test" appears on screen while the instrument is performing the test. When the test is finished, the message "Disk Test complete" will appear on screen.
3. If you are running repetitive tests, press the front-panel STOP key when you want to discontinue the test. The number of runs and failures will be displayed in the menu.
4. To return to HP 1652B/1653B Self Tests menu, move the cursor to **Done** and press SELECT.

Cycle Through Tests

Cycle through tests allows you to cycle through the following tests:

- Analyzer Data Acquisition
- Scope Data Acquisition
- BNC
- RAM
- ROM
- Disk Drive

1. In HP 1652B/1653B Self Tests menu, move the cursor to **Cycle through tests** and press SELECT.

   The tests listed above will run consecutively and continually until the front-panel STOP key is pressed.

2. Press the front-panel STOP key to end the continuous tests.

3. To see the results of the tests for individual tests, move the cursor to the appropriate test and press SELECT. The number of runs and failures of the continuous test will be displayed on the individual self test menu.

4. Move the cursor to **Done** and press SELECT to return to the HP 1652B/1653B Self Tests menu.

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6C

Troubleshooting

Introduction

This section provides troubleshooting information for the HP 1652B/1653B Logic Analyzer. Troubleshooting consists of flowcharts, and signal level tables. The troubleshooting information is provided to isolate a faulty assembly. When a faulty assembly has been located, the disassembly/assembly procedures in section 6D help direct replacement of the assembly.

Self-test descriptions and instructions are provided in section 6B.

Caution

The effects of ELECTROSTATIC DISCHARGE can damage electronic components. Use grounded wriststraps and mats when performing any kind of service to this instrument.

Safety

Read the Safety Summary at the front of this manual before servicing the instrument. Before performing any procedure, review it for cautions and warnings.

Warning

Maintenance should be performed by trained service personnel aware of the hazards involved (for example, fire and electric shock). When maintenance can be performed without power applied, the power cord should be removed from the instrument.

Trouble Isolation Flowcharts

The trouble isolation flowcharts are the troubleshooting guides. Start there when repairing a defective instrument.

The flowcharts refer to other tests, tables, and procedures to help isolate troubles. Disassembly procedures are included in section 6D to direct you in replacing faulty assemblies. The circled numbers on the charts indicate the next chart to use for isolating a problem.

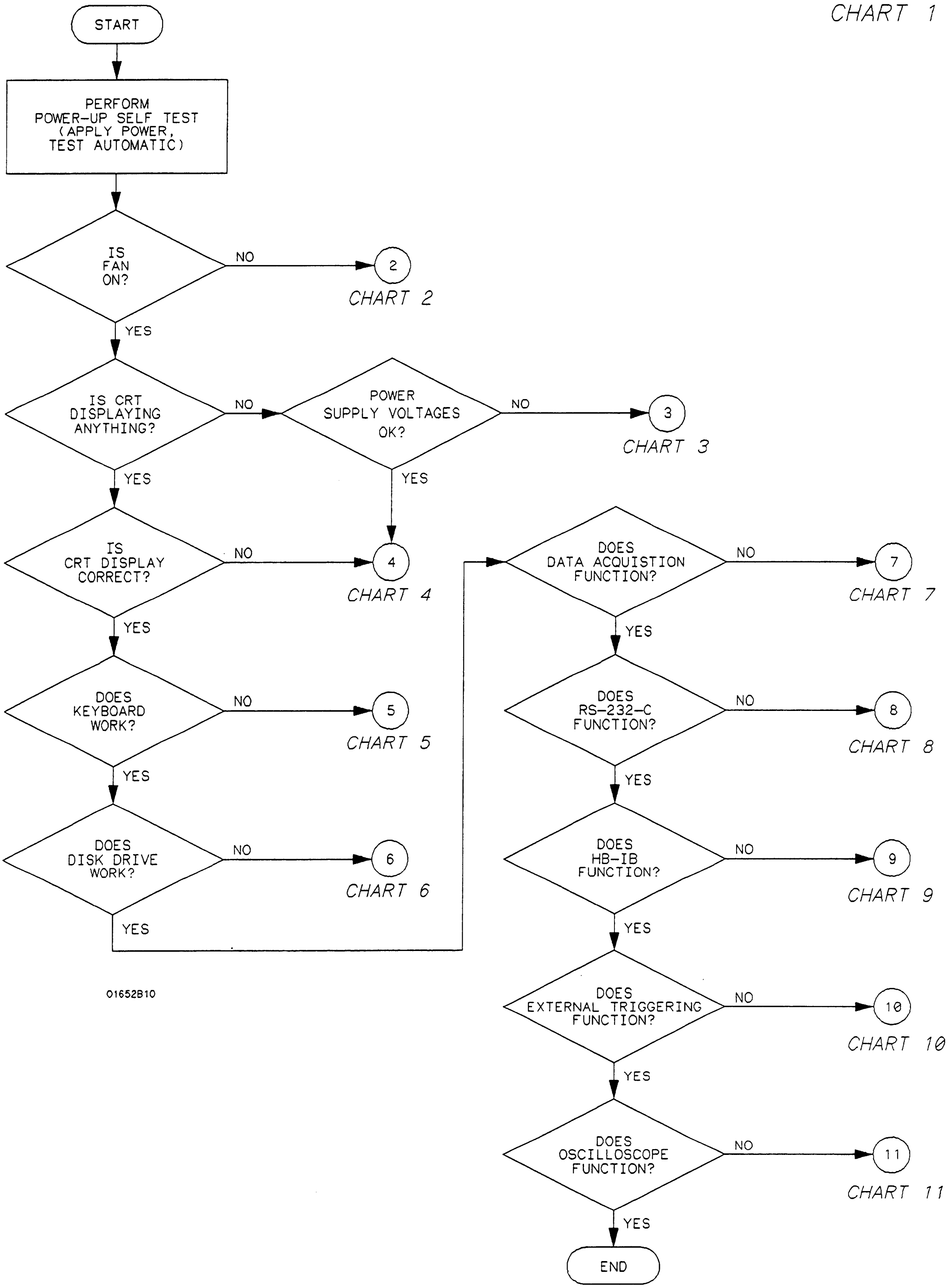


CHART 1
START
PERFORM POWER-UP SELF TEST (APPLY POWER, TEST AUTOMATIC)
IS FAN ON?
NO
2
CHART 2
YES
IS CRT DISPLAYING ANYTHING?
NO
POWER SUPPLY VOLTAGES OK?
NO
3
CHART 3
YES
YES
IS CRT DISPLAY CORRECT?
NO
4
CHART 4
YES
DOES KEYBOARD WORK?
NO
5
CHART 5
YES
DOES DISK DRIVE WORK?
NO
6
CHART 6
YES
DOES DATA ACQUISTION FUNCTION?
NO
7
CHART 7
YES
DOES RS-232-C FUNCTION?
NO
8
CHART 8
YES
DOES HB-IB FUNCTION?
NO
9
CHART 9
YES
DOES EXTERNAL TRIGGERING FUNCTION?
NO
10
CHART 10
YES
DOES OSCILLOSCOPE FUNCTION?
NO
11
CHART 11
YES
END
01652B10

Figure 6C-1. Primary Troubleshooting Flowchart

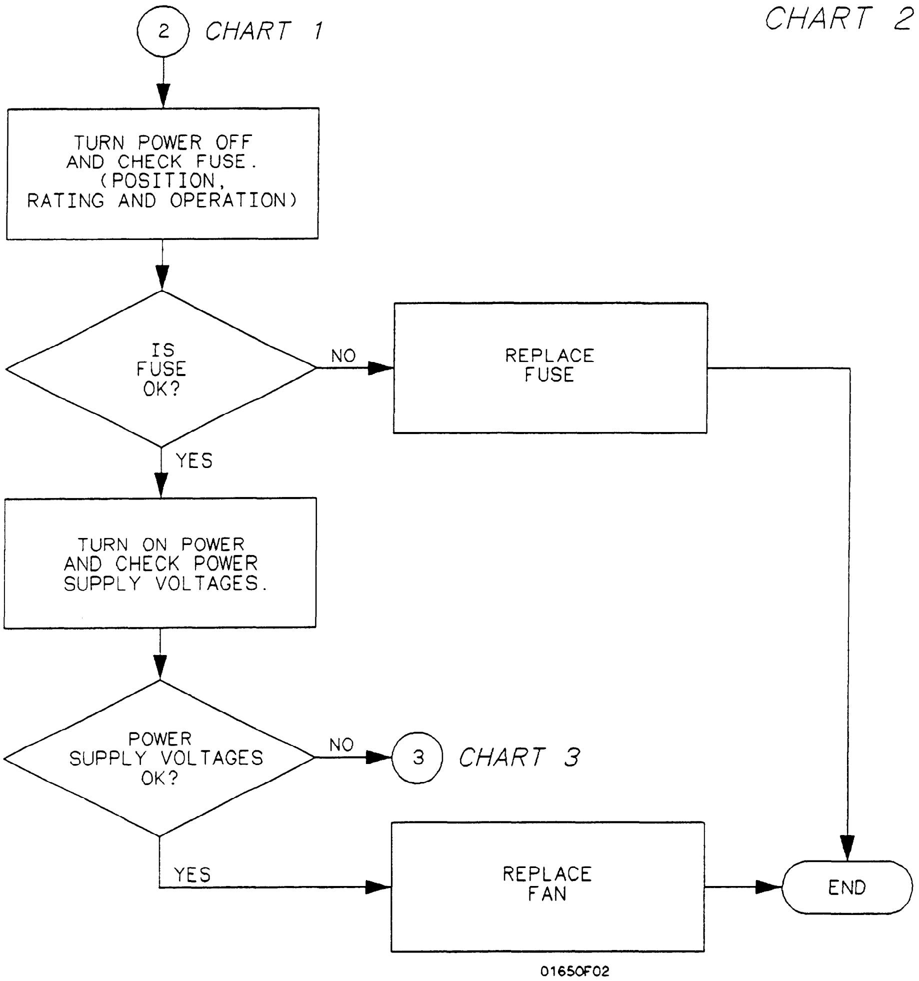
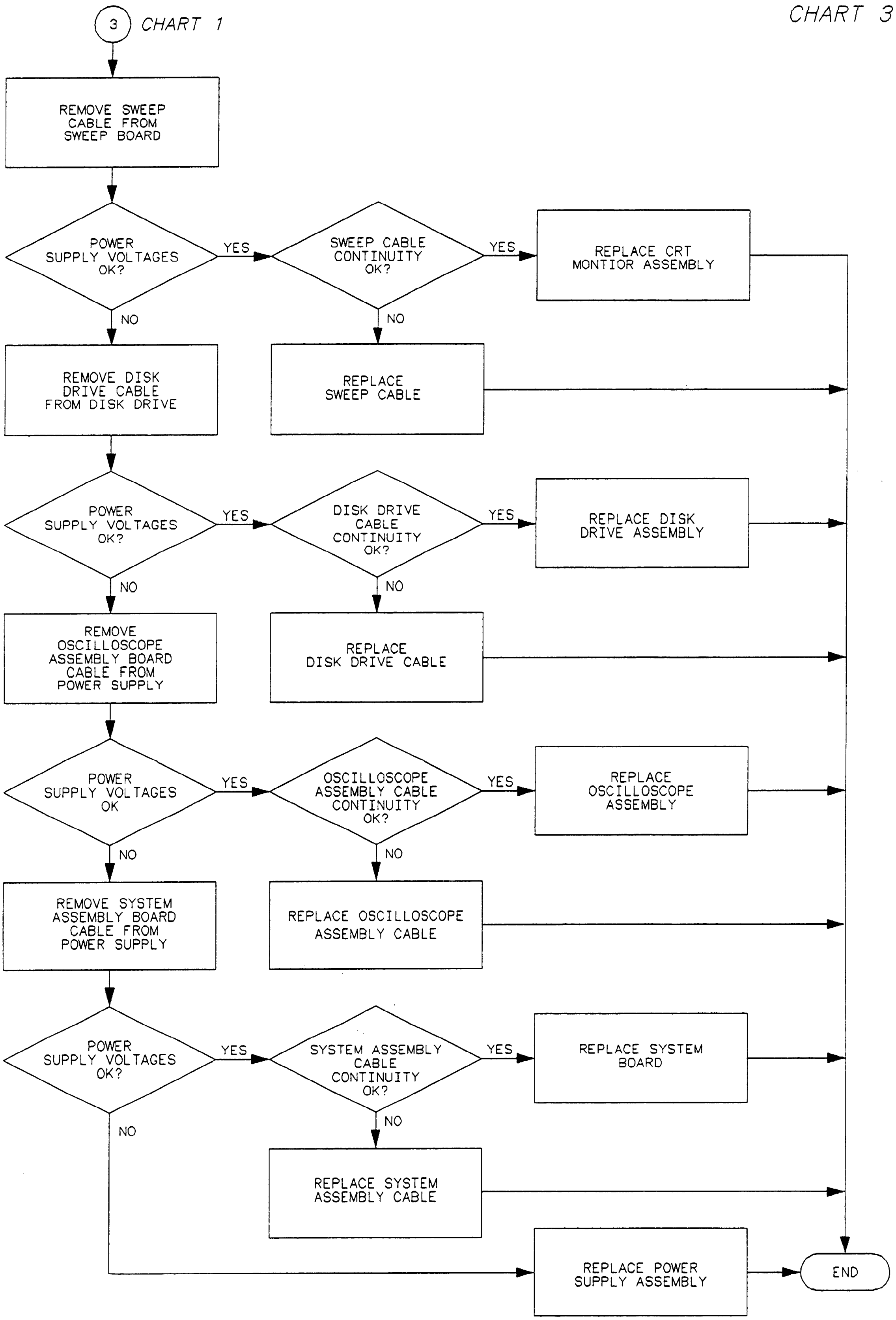
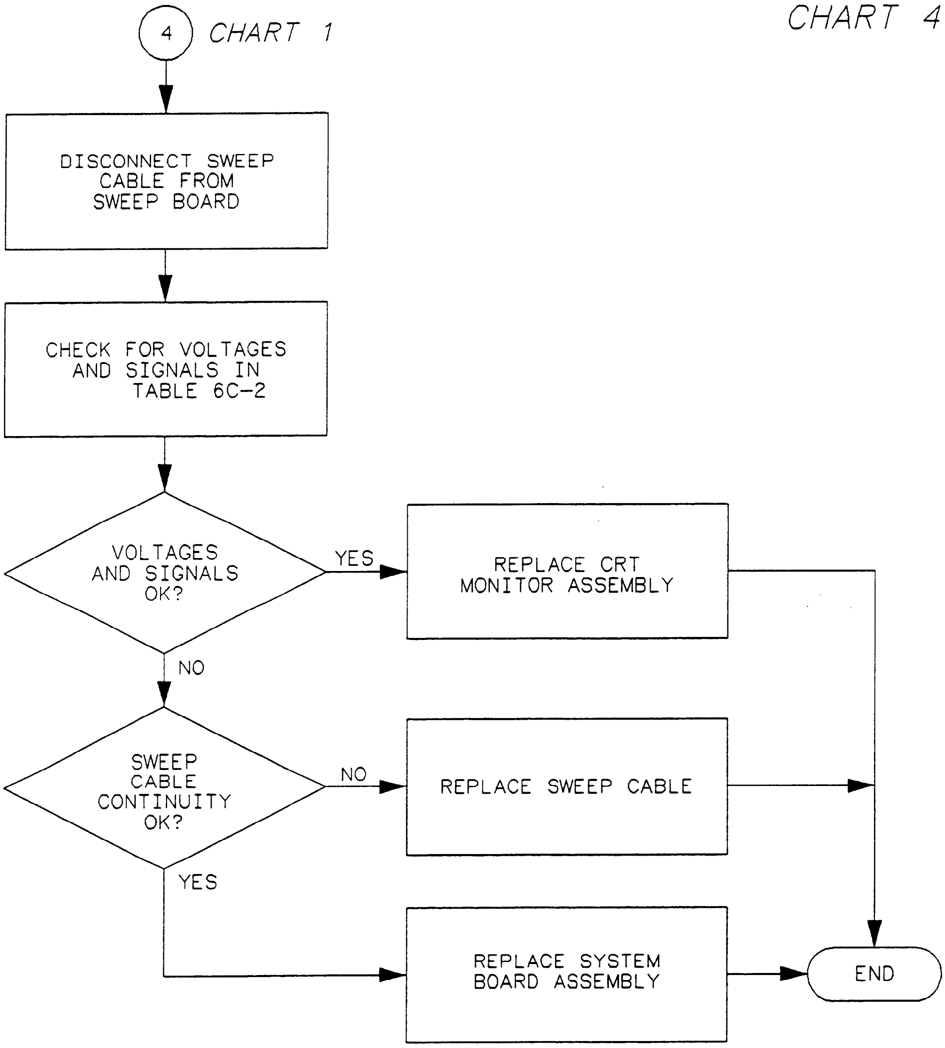

2
CHART 1
CHART 2
TURN POWER OFF AND CHECK FUSE. (POSITION, RATING AND OPERATION)
IS FUSE OK?
NO
REPLACE FUSE
YES
TURN ON POWER AND CHECK POWER SUPPLY VOLTAGES.
POWER SUPPLY VOLTAGES OK?
NO
3
CHART 3
YES
REPLACE FAN
END
01650F02

Figure 6C-2. Trouble Isolation Flowchart for Fan/Fuse



3 CHART 1
CHART 3
REMOVE SWEEP CABLE FROM SWEEP BOARD
POWER SUPPLY VOLTAGES OK?
YES
NO
SWEEP CABLE CONTINUITY OK?
REPLACE CRT MONTIOR ASSEMBLY
REMOVE DISK DRIVE CABLE FROM DISK DRIVE
REPLACE SWEEP CABLE
POWER SUPPLY VOLTAGES OK?
DISK DRIVE CABLE CONTINUITY OK?
REPLACE DISK DRIVE ASSEMBLY
REMOVE OSCILLOSCOPE ASSEMBLY BOARD CABLE FROM POWER SUPPLY
REPLACE DISK DRIVE CABLE
POWER SUPPLY VOLTAGES OK
OSCILLOSCOPE ASSEMBLY CABLE CONTINUITY OK?
REPLACE OSCILLOSCOPE ASSEMBLY
REMOVE SYSTEM ASSEMBLY BOARD CABLE FROM POWER SUPPLY
REPLACE OSCILLOSCOPE ASSEMBLY CABLE
POWER SUPPLY VOLTAGES OK?
SYSTEM ASSEMBLY CABLE CONTINUITY OK?
REPLACE SYSTEM BOARD
REPLACE SYSTEM ASSEMBLY CABLE
REPLACE POWER SUPPLY ASSEMBLY
END

Figure 6C-3. Trouble Isolation for Power Supply


4
CHART 1
DISCONNECT SWEEP CABLE FROM SWEEP BOARD
CHECK FOR VOLTAGES AND SIGNALS IN TABLE 6C-2
VOLTAGES AND SIGNALS OK?
YES
REPLACE CRT MONITOR ASSEMBLY
NO
SWEEP CABLE CONTINUITY OK?
NO
REPLACE SWEEP CABLE
YES
REPLACE SYSTEM BOARD ASSEMBLY
END

01652B13

Figure 6C-4. Trouble Isolation for CRT Monitor

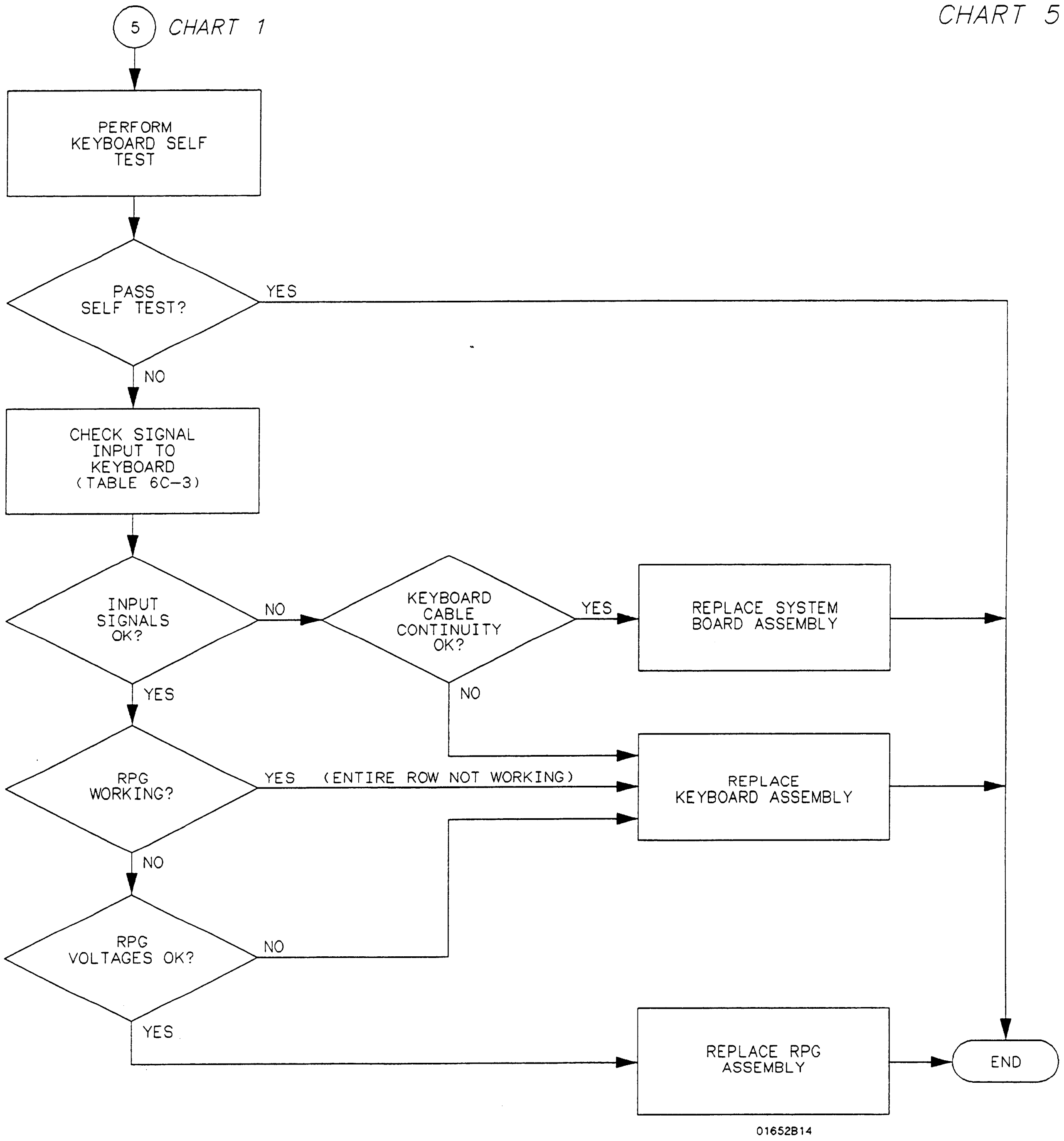

5
CHART 1
PERFORM KEYBOARD SELF TEST
PASS SELF TEST?
YES
NO
CHECK SIGNAL INPUT TO KEYBOARD (TABLE 6C-3)
INPUT SIGNALS OK?
NO
KEYBOARD CABLE CONTINUITY OK?
YES
REPLACE SYSTEM BOARD ASSEMBLY
NO
YES
RPG WORKING?
YES (ENTIRE ROW NOT WORKING)
REPLACE KEYBOARD ASSEMBLY
NO
RPG VOLTAGES OK?
NO
YES
REPLACE RPG ASSEMBLY
END
01652B14

Figure 6C-5. Trouble Isolation for Keyboard

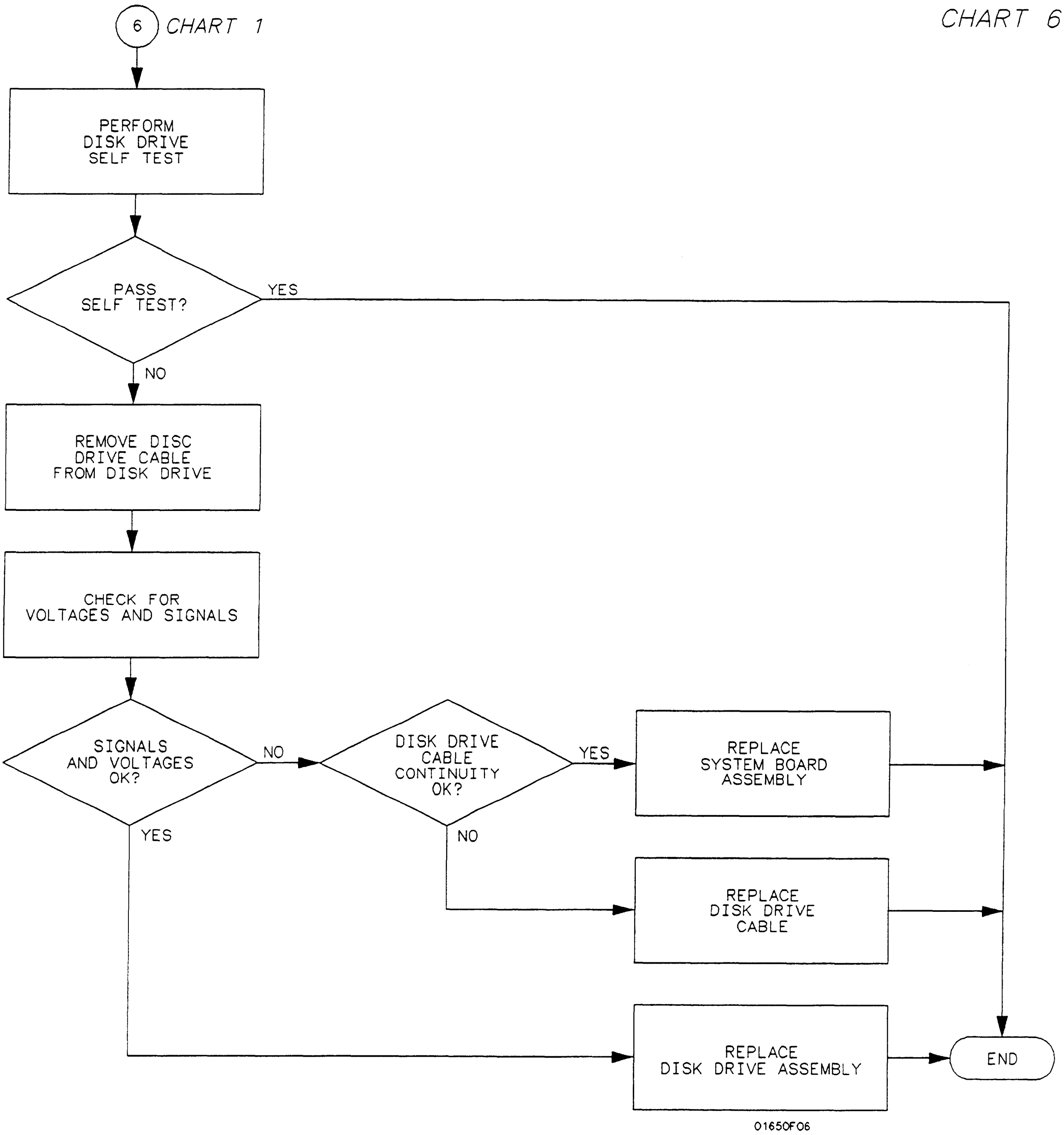
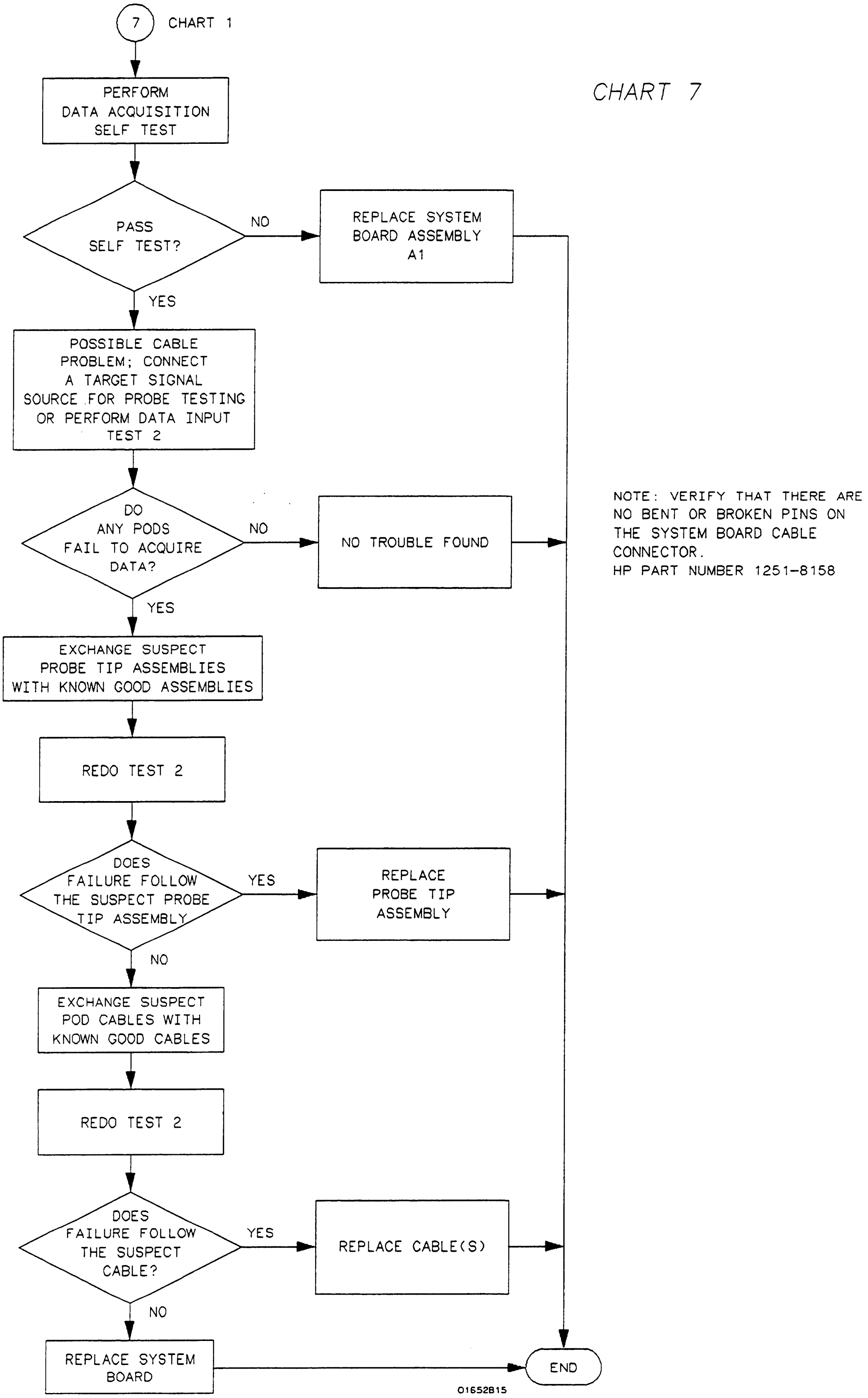

6
CHART 1
PERFORM DISK DRIVE SELF TEST
PASS SELF TEST?
YES
NO
REMOVE DISC DRIVE CABLE FROM DISK DRIVE
CHECK FOR VOLTAGES AND SIGNALS
SIGNALS AND VOLTAGES OK?
NO
YES
DISK DRIVE CABLE CONTINUITY OK?
YES
NO
REPLACE SYSTEM BOARD ASSEMBLY
REPLACE DISK DRIVE CABLE
REPLACE DISK DRIVE ASSEMBLY
END
01650F06

Figure 6C-6. Trouble Isolation for Disk Drive


7
CHART 1
CHART 7
PERFORM DATA ACQUISITION SELF TEST
PASS SELF TEST?
NO
REPLACE SYSTEM BOARD ASSEMBLY A1
YES
POSSIBLE CABLE PROBLEM; CONNECT A TARGET SIGNAL SOURCE FOR PROBE TESTING OR PERFORM DATA INPUT TEST 2
DO ANY PODS FAIL TO ACQUIRE DATA?
NO
NO TROUBLE FOUND
YES
EXCHANGE SUSPECT PROBE TIP ASSEMBLIES WITH KNOWN GOOD ASSEMBLIES
REDO TEST 2
DOES FAILURE FOLLOW THE SUSPECT PROBE TIP ASSEMBLY
YES
REPLACE PROBE TIP ASSEMBLY
NO
EXCHANGE SUSPECT POD CABLES WITH KNOWN GOOD CABLES
REDO TEST 2
DOES FAILURE FOLLOW THE SUSPECT CABLE?
YES
REPLACE CABLE(S)
NO
REPLACE SYSTEM BOARD
END
01652B15

NOTE: VERIFY THAT THERE ARE NO BENT OR BROKEN PINS ON THE SYSTEM BOARD CABLE CONNECTOR.
HP PART NUMBER 1251-8158

Figure 6C-7. Trouble Isolation for Data Acquisition

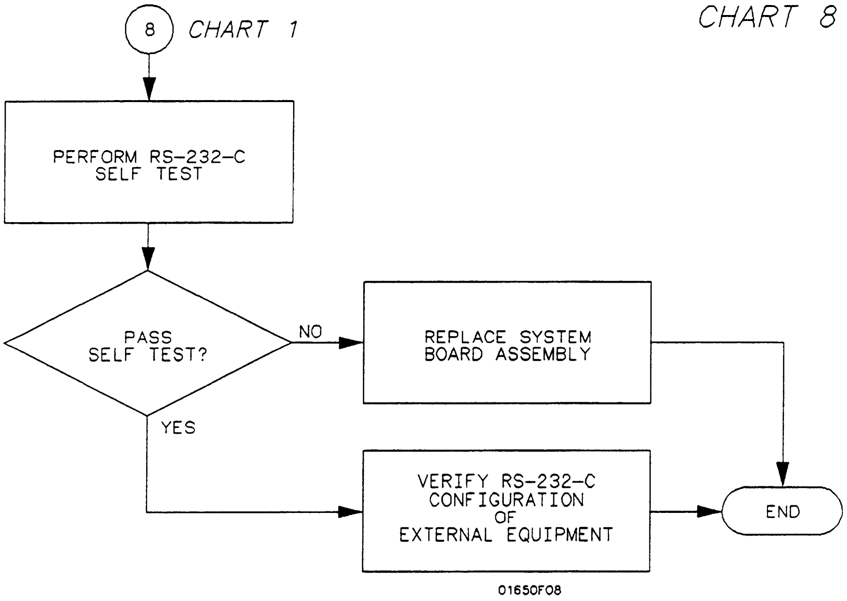

8
CHART 1
CHART 8
PERFORM RS-232-C SELF TEST
PASS SELF TEST?
NO
REPLACE SYSTEM BOARD ASSEMBLY
YES
VERIFY RS-232-C CONFIGURATION OF EXTERNAL EQUIPMENT
END
01650F08

Figure 6C-8. Trouble Isolation for RS-232C

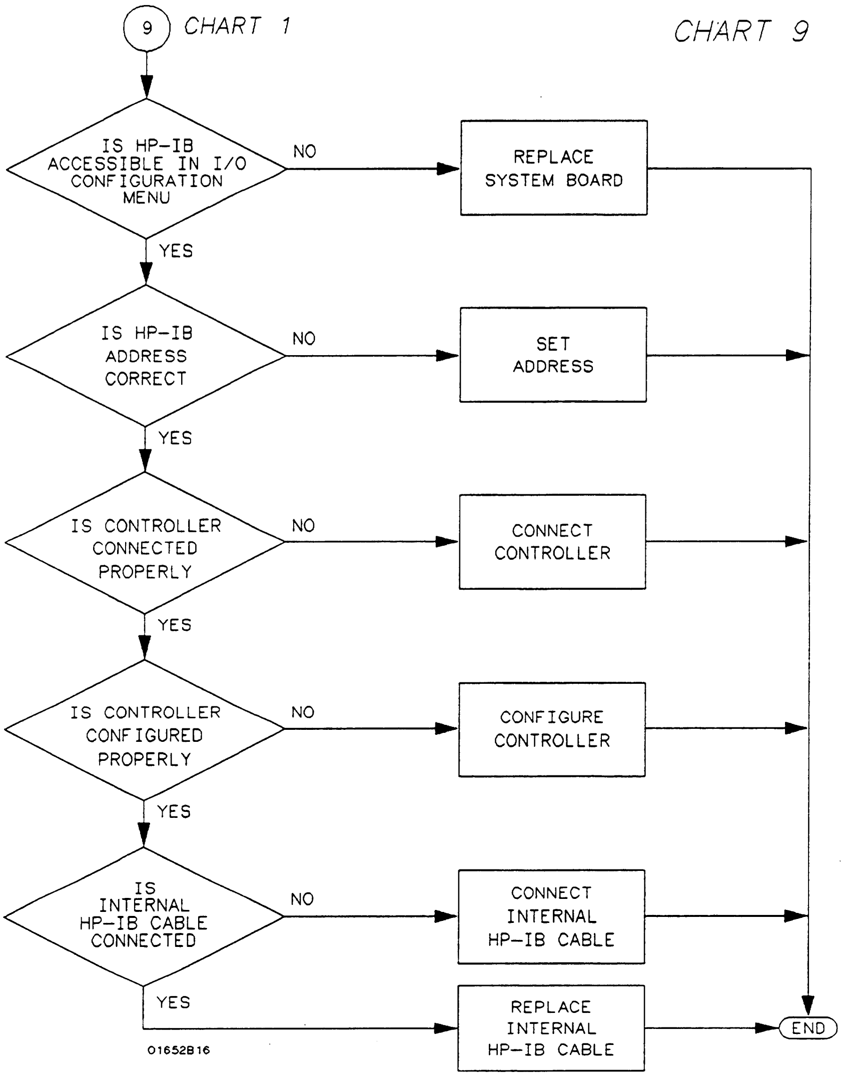

9
CHART 1
CHART 9
IS HP-IB ACCESSIBLE IN I/O CONFIGURATION MENU
NO
REPLACE SYSTEM BOARD
YES
IS HP-IB ADDRESS CORRECT
NO
SET ADDRESS
YES
IS CONTROLLER CONNECTED PROPERLY
NO
CONNECT CONTROLLER
YES
IS CONTROLLER CONFIGURED PROPERLY
NO
CONFIGURE CONTROLLER
YES
IS INTERNAL HP-IB CABLE CONNECTED
NO
CONNECT INTERNAL HP-IB CABLE
YES
REPLACE INTERNAL HP-IB CABLE
END
01652B16

Figure 6C-9. Trouble Isolation for HP-IB

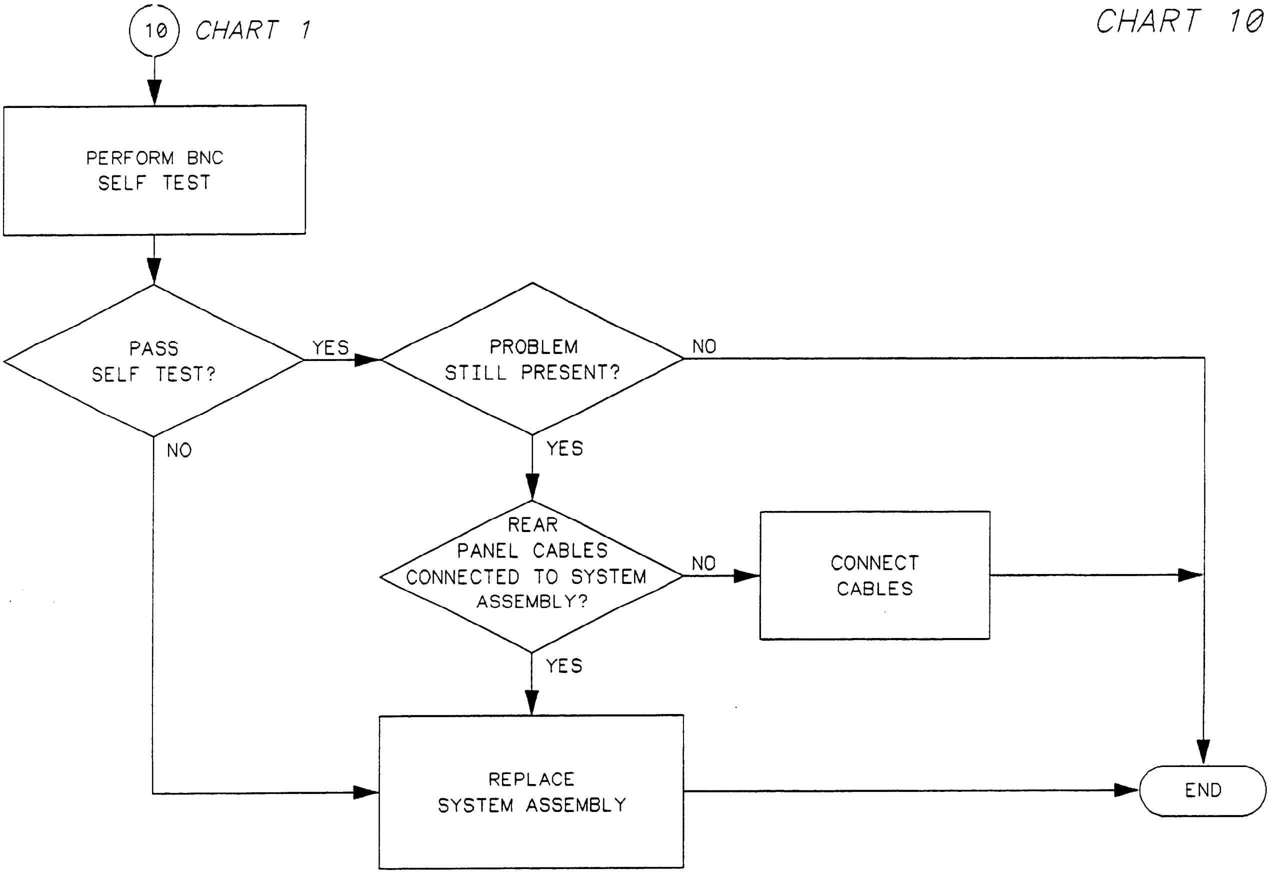

10
CHART 1
PERFORM BNC SELF TEST
PASS SELF TEST?
YES
NO
PROBLEM STILL PRESENT?
NO
YES
REAR PANEL CABLES CONNECTED TO SYSTEM ASSEMBLY?
NO
YES
CONNECT CABLES
REPLACE SYSTEM ASSEMBLY
END

Figure 6C-10. Trouble Isolation for BNC

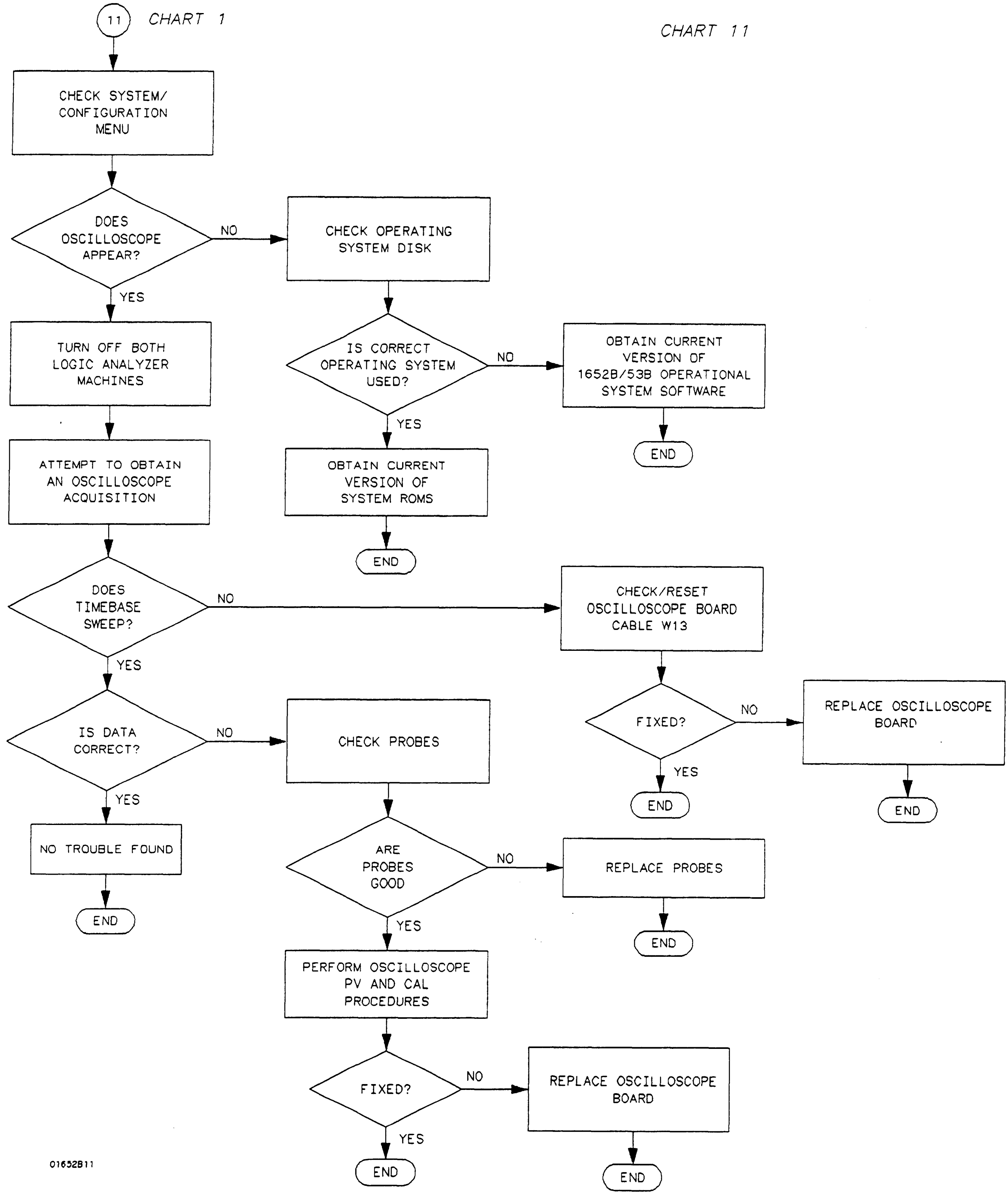

11
CHART 1
CHART 11
CHECK SYSTEM/ CONFIGURATION MENU
DOES OSCILLOSCOPE APPEAR?
NO
CHECK OPERATING SYSTEM DISK
YES
TURN OFF BOTH LOGIC ANALYZER MACHINES
IS CORRECT OPERATING SYSTEM USED?
NO
OBTAIN CURRENT VERSION OF 1652B/53B OPERATIONAL SYSTEM SOFTWARE
END
YES
ATTEMPT TO OBTAIN AN OSCILLOSCOPE ACQUISITION
OBTAIN CURRENT VERSION OF SYSTEM ROMS
END
DOES TIMEBASE SWEEP?
NO
CHECK/RESET OSCILLOSCOPE BOARD CABLE W13
YES
FIXED?
NO
REPLACE OSCILLOSCOPE BOARD
YES
END
END
IS DATA CORRECT?
NO
CHECK PROBES
YES
NO TROUBLE FOUND
END
ARE PROBES GOOD
NO
REPLACE PROBES
END
YES
PERFORM OSCILLOSCOPE PV AND CAL PROCEDURES
FIXED?
NO
REPLACE OSCILLOSCOPE BOARD
YES
END
END
01652B11

Figure 6C-11. Trouble Isolation for Oscilloscope

Power Supply Voltages Check

The power supply must be loaded by either the System Assembly Board or with an added resistor to check the voltages.

Warning

This procedure is to be performed only by service-trained personnel aware of the hazards involved (such as fire and electrical shock).

Power Supply Loaded by System Assembly

1. Remove the instrument top cover.
2. Using the figure below, check for the voltages indicated at the testpoints.

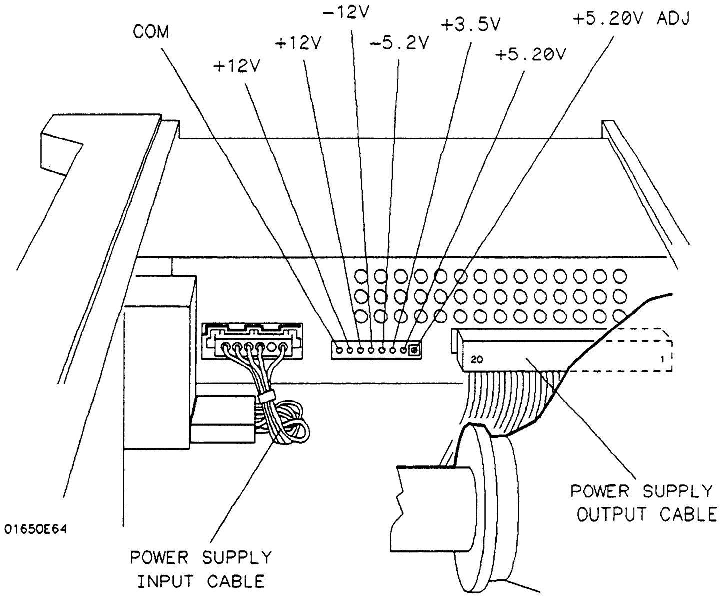


Figure 6C-12. Power Supply Test Points

Power Supply Isolated

Isolate and check the supply with the following steps. Use the figure above for reference.

1. Turn off the instrument and remove the power cable.
2. Disconnect the supply output cable at the supply (see figure above).
3. Load the +5.20 V supply with a 2 ohm 25 watt resistor.
    a. With a jumper wire, connect one end of the resistor to one of the 5.20 V pins (pins 1 through 4) on the supply output.
    b. With another jumper wire, connect the other end of the resistor to one of the ground pins (pins 5 through 8) on the supply output.

4. Reconnect the power cable and turn on the instrument. Then check for the voltages at the supply output using the values in the following table.

Table 6C-2. Power Supply/Main Assembly Voltages

PIN	SIGNAL	PIN	SIGNAL
1	+5.20 V	11	-5.2 V
2	+5.20 V	12	GROUND
3	+5.20 V	13	+12 V
4	+5.20 V	14	GROUND
5	GROUND (Display)	15	-12 V
6	GROUND (Digital)	16	GROUND
7	GROUND (Digital)	17	+12 V (Display)
8	GROUND (Display)	18	-5.2 V
9	+3.5 V	19	+15.5 V (Fan)
10	GROUND	20	GROUND (Fan)

Note The ground planes (digital, fan, and display) are at the same potential on the power supply, but when you are measuring them on the main assembly, the supplies must be measured with reference to the respective ground.

CRT Monitor Signals Check

1. Remove the instrument top cover.
2. Check the CRT Monitor input cable for the signals and supplies listed in the table below. The cable is the wide ribbon cable connecting the monitor assembly to the System Assembly Board.
3. Dynamic video signals FB (Full-bright) and HB (Half-bright) are TTL inputs. Check for activity on these lines. The table includes a truth table for these signals.

Table 6C-1. CRT Monitor Input Cable Pin Assignments

PIN	SIGNAL	PIN	SIGNAL
1	+5 V (Digital)	2	+12 V (Display)
3	GROUND (Display)	4	GROUND (Display)
5	+12 V (Display)	6	GROUND (Display)
7	+12 V (Display)	8	GROUND (Display)
9	+12 V (Display)	10	HSYNC
11	VSYNC	12	+12 V (Display)
13	GROUND (Digital)	14	GROUND (Digital)
15	GROUND (Display)	16	FB (Full-bright)
17	GROUND (Display)	18	HB (Half-bright)
19	GROUND (Display)	20	+5 V (Digital)

FB	HB	VIDEO
0	0	OFF
0	1	HALF
1	0	FULL
1	1	FULL

Keyboard Signals Check

Isolate a faulty elastomeric keypad or keyboard when the random key(s) are not operating by performing the following steps.

1. Turn off the instrument and remove the power cable.
2. Without disconnecting the keyboard cable, follow the keyboard removal procedure to loosen the keyboard. Leave the keyboard in place in front of the instrument.
3. Reconnect the power cable and turn on the instrument.
4. Run the Keyboard Self Test and press all of the keys.
5. Allow the keyboard assembly to fall forward from the front panel. Separate the elastomeric keypad and keyboard panel from the PC board.
6. Short the PC board trace (with a paper clip or screwdriver) of the non-operating key and look for an appropriate response on the display.
7. If the display responds as if the key were pressed, replace the elastomeric keypad.
8. If the display does not respond as if the key were pressed, replace the keyboard.

The RPG connector has a TTL pulse on pins 1 and 3, when the knob is being turned. Pin 5 of the connector is + 5 V.

The ROW (scan) signal is a low duty-cycle pulse at approximately 60 Hz. It is continually present on pins 14 through 20 of the keyboard cable. Because of the resistance of the keypad contacts, the signal does not appear the same on the COLUMN (data) pins when keys are pressed. Refer to the following table for signals going to and from the keyboard.

Table 6C-3. Keyboard Connector Voltages and Signals

PIN	SIGNAL	PIN	SIGNAL
1	GROUND	2	GROUND
3	COLUMN 6 (Data)	4	+5 V (DIGITAL)
5	GROUND	6	RPG (CLICKS)
7	RPG (DIRECTION)	8	N/C
9	COLUMN 5 (Data)	10	COLUMN 4 (Data)
11	COLUMN 3 (DATA)	12	COLUMN 2 (DATA)
13	COLUMN 1 (DATA)	14	ROW 4 (Scan)
15	ROW 5 (Scan)	16	ROW 2 (Scan)
17	ROW 3 (Scan)	18	ROW 1 (Scan)
19	ROW 0 (SCAN)	20	ROW 6 (SCAN)

Disk Drive Voltages Check

Use the following steps to check the disk drive voltages.

1. Remove the top cover of the instrument.
2. Run the repetitive Disk Drive Self Test.
3. Remove the disk drive cable from the disk drive.
4. Check the disk drive cable for the voltages listed in the following table.

PIN	SIGNAL DESCRIPTION	PIN	SIGNAL DESCRIPTION
1	CHANGE RESET (+5 V)	2	DISK CHANGE
3	+5 V	4	IN USE
5	+5 V	6	DRIVE SELECT3 (+5 V)
7	+5 V	8	INDEX
9	+5 V	10	DRIVE SELECT0
11	+5 V	12	DRIVE SELECT1
13	GROUND	14	DRIVE SELECT2 (+5 V)
15	GROUND	16	MOTOR ON
17	GROUND	18	DIRECTION
19	GROUND	20	STEP
21	GROUND	22	WRITE DATA
23	GROUND	24	WRITE GATE
25	GROUND	26	TRACK 00
27	GROUND	28	WRITE PROTECT
29	+12 V	30	READ DATA
31	+12 V	32	HEAD SELECT
33	+12 V	34	READY

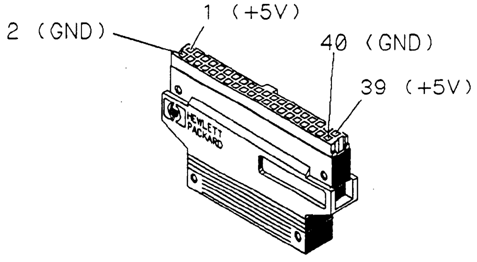
Caution ✋

Do not match the arrows of the cable and connector when connecting the disk drive cable to the disk drive. The connector of the disk drive is marked with an arrow at pin 34 of the connector. The end of the disk drive cable is marked at pin 1 of the cable. Matching the arrows will damage the disk drive.

Troubleshooting Auxiliary Power

The +5 volt auxiliary power line is protected by a current limiting circuit. If the current on pins 1 and 39 exceeds 2.3 amperes, the circuit will open. When the short is removed, the circuit will reset in approximately 20 ms. If you suspect a problem with this circuit, remove all loads from pins 1 and 39 and measure the voltage between these pins and ground (pins 2 and 40) with a voltmeter. There should be +5 volts at pins 1 and 39 after the 20 ms reset time.

If the +5 volts does not appear on one or both of these pins (pins 1 and 39), replace the analyzer cable. If the +5 volts still does not appear on these pins, refer to chart 3 in figure 6C-3.



01650E67

Figure 6C-13. Cable Power and Ground

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6D

Assembly Removal and Replacement

Introduction

This section contains the procedures for removal and installation of major assemblies of the HP 1652B/1653B Logic Analyzer. Read the Safety Summary at the front of this manual before servicing the instrument. The relative location of the replaceable components are shown in figure 6D-1. The part numbers and descriptions for these components are listed in section 5.

Warning

Hazardous voltages exist on the power supply, the CRT, and the display sweep board. To avoid electrical shock, adhere closely to the following procedures. After disconnecting the power cable, wait at least three minutes for the capacitors on the power supply and sweep boards to discharge before servicing this instrument.

Caution

Never attempt to remove or install any assembly with the instrument ON or the power cable connected. This can result in component damage.

Caution

The effects of ELECTROSTATIC DISCHARGE can damage electronic components. Use grounded wriststraps and mats when performing any kind of service to this instrument.

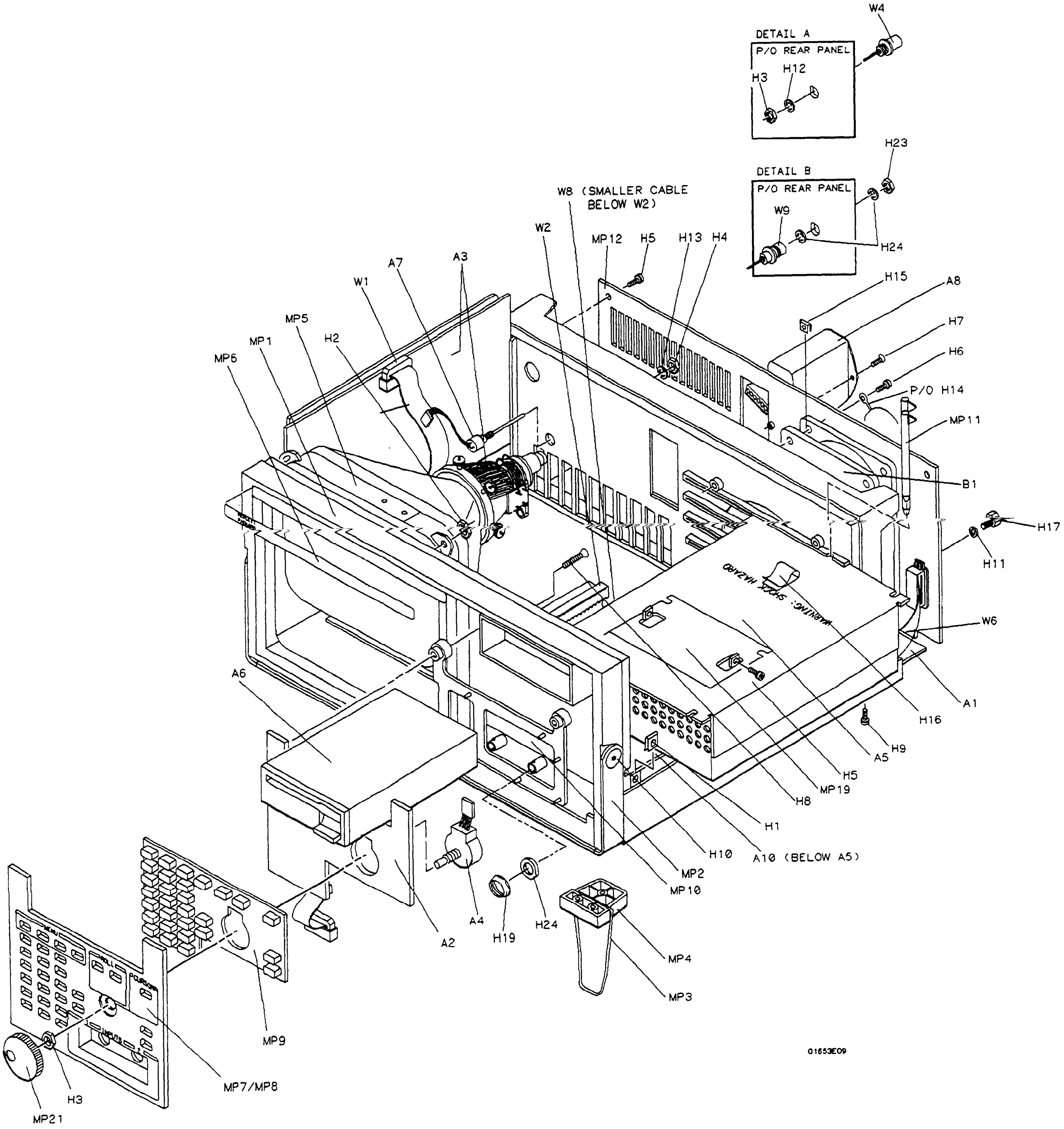
W4
DETAIL A
P/O REAR PANEL
H3
H12
H23
DETAIL B
P/O REAR PANEL
W9
H24
W8 (SMALLER CABLE BELOW W2)
W2
MP12
H5
H13
H4
H15
A8
A7
A3
W1
MP5
MP1
H2
MP6
H7
H6
P/O H14
MP11
B1
H17
H11
W6
A1
H16
H9
A5
H5
MP19
H8
H1
H10
A10 (BELOW A5)
MP2
MP10
A6
A4
H19
H24
A2
MP4
MP3
MP9
MP7/MP8
H3
MP21
01653E09

Figure 6D-1. HP 1652B/1653B Exploded View

Removal and Replacement of the Rear Panel Assembly

1. Turn off the instrument and disconnect the power cable.
2. Disconnect the logic analyzer cables from the rear panel of the instrument.
3. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
4. Lift off the top cover.
5. Disconnect the line filter cable from the power supply.
6. Disconnect the ground cable of the line filter from the oscilloscope assembly.
7. Disconnect the Intensity adjust cable from the rear of the high voltage sweep board.
8. Remove the eight screws at the edges of the rear panel.
9. Pull the rear panel straight out from the instrument about three inches.

Note

An ESD ground spring clip is installed on the RS-232C connector behind the rear panel. This ground spring clip is not mechanically secured to the instrument. Make sure the ground spring clip does not fall off during disassembly.

---

10. Remove the two screws holding the HP-IB ribbon cable connector to the rear panel.
11. Disconnect the External Trigger Input cable from connector J9 on the Main Assembly.
12. Disconnect the External Trigger Output cable from connector J10 on the Main Assembly.
13. Disconnect the Probe Compensation cable from the oscilloscope board.
14. Disconnect the fan cable from the Main Assembly.
15. Separate the rear panel from the instrument cabinet.
16. Replace the rear panel by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the Disk Drive

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the two screws securing the disk drive to the power supply panel.
5. Disconnect the disk drive cable assembly (W3) from the disk drive.

Caution

Do not match the arrows of the cable and connector when reconnecting the disk drive cable to the disk drive. The connector of the disk drive is marked with an arrow at pin 34 of the connector. The end of the disk drive cable is marked at pin 1 of the cable. Matching the arrows will result in damaging the disk drive.

---

6. Slide the disk drive through the front panel of the instrument cabinet as in figure 6D-2.
7. Replace the disk drive by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

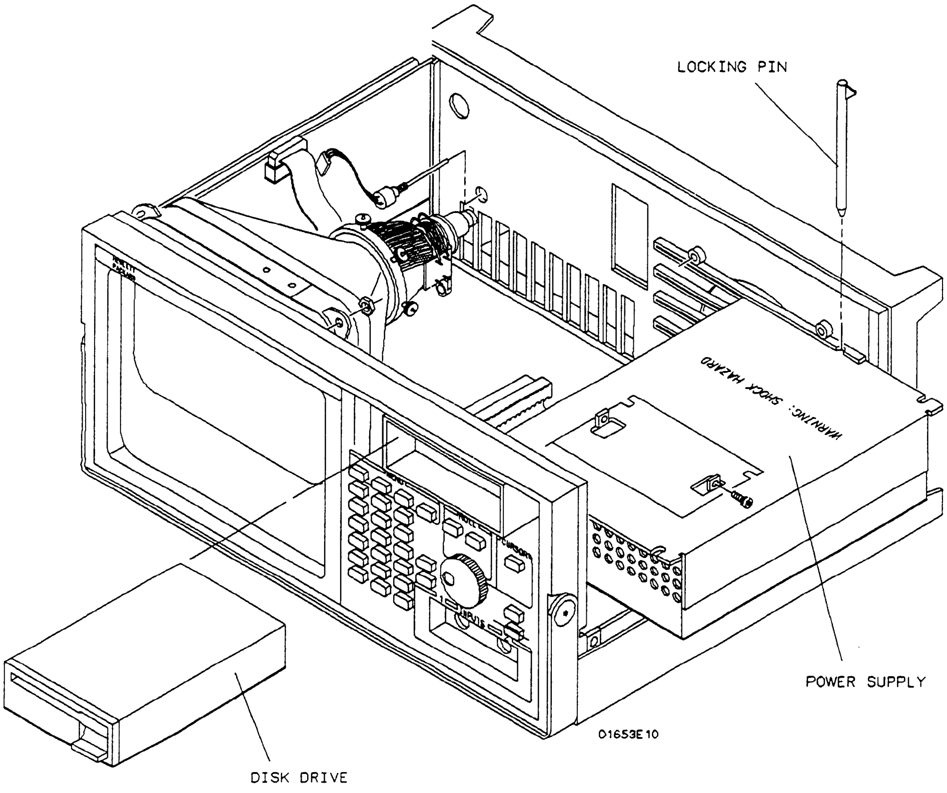

Figure 6D-2. Disk Drive and Power Supply Removal

Removal and Replacement of the Power Supply Assembly

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Disk Drive
5. Remove the disk drive cable assembly (W3) from the disk drive panel and let it lay off the side of the instrument.
6. Remove the cable (W2) that connects the Power Supply to the Main Assembly.
7. Disconnect the line filter cable from the Power Supply.
8. Remove the two locking pins that secure the Power Supply at the right front and rear corners of the instrument cabinet. Pull these pins up and out of the instrument.
9. Slide the power supply through the side of the cabinet as in the previous figure 6D-2.
10. Replace the power supply by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the Oscilloscope Assembly

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Disk Drive and Power Supply.
5. Remove the Line Filter Switch Assembly from the rear panel.
6. Disconnect the probe compensation cable from the oscilloscope assembly.
7. Disconnect the ground cable of the line filter from the oscilloscope assembly.
8. Disconnect the cable assembly W8 from connector J2 on the oscilloscope assembly.

9. Remove the six screws securing the oscilloscope assembly to the support panel.

Note

Do not remove the two screws at the front of the oscilloscope board that hold the two attenuators in place.

---

10. Remove the two nuts (H19) and two washers (H20) that secure the attenuator BNCs to the front panel.
11. Slide the oscilloscope assembly toward the rear panel to allow the BNCs to clear the front panel.
12. Remove the oscilloscope assembly by tilting the rear of the assembly up and lifting the assembly out through the top of the instrument cabinet. Make sure that the BNCs clear the front panel.
13. Replace the oscilloscope assembly by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

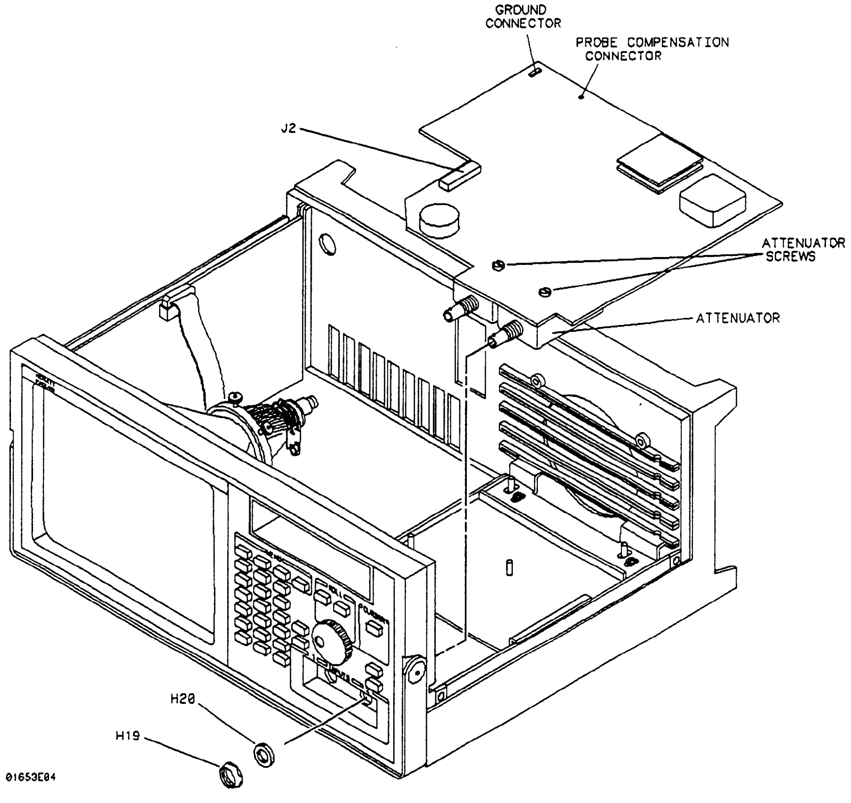

Figure 6D-3. Oscilloscope Assembly Removal

Removal and Replacement of the Attenuators

Attenuators are not part of the oscilloscope board. If the oscilloscope board is replaced, the attenuators must be moved to the replacement board.

Caution

ELECTROSTATIC DISCHARGE can damage electronic components. Use grounded wriststraps and mats when servicing attenuators.

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Disk Drive, Power Supply, and Oscilloscope Assembly.
5. From the component side of the Oscilloscope Assembly, remove the two screws that secure the Attenuator.
6. A 24-pin connector, located at the rear of the inside of the attenuator, connects the attenuator to the PC board. With a gentle rocking or prying motion, lift the attenuator from the PC board.

Note

Prying at the rear of the attenuator with a small flat-blade screwdriver, between the attenuator and the PC board, will help control the attenuator removal.

7. Replace the attenuator by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the Keyboard Assembly

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Disk Drive, Power Supply, and Oscilloscope Assembly.
5. Loosen the two screws that hold the rear bracket on the oscilloscope assembly support panel until the bracket moves freely.
6. Remove the support panel by carefully tilting the rear of the panel up and lifting the panel out through the top of the instrument cabinet. Make sure the metal tabs on the front of the support panel clear the front panel.

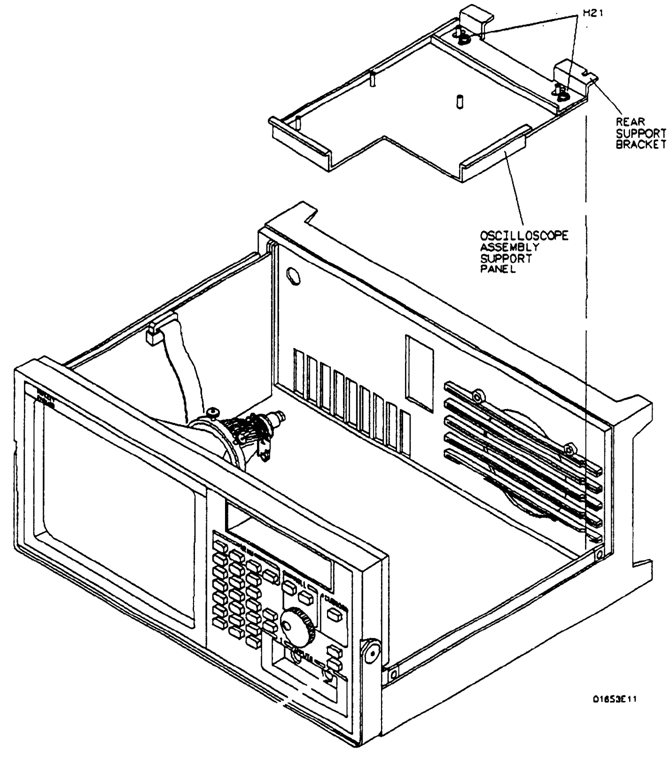

Figure 6D-4. Support Panel Removal

7. From the back side of the front panel, remove the four screws securing the keyboard assembly to the front of the instrument cabinet.
8. Disconnect the keyboard assembly ribbon cable from the Main Assembly.
9. Pull on the knob to remove the keyboard assembly (label, keyboard panel, keypad, PC board, RPG, and knob) from the front panel as one unit.

Disassembling the Keyboard Assembly

Use the following steps to disassemble the keyboard assembly.

10. Disconnect the Rotary Pulse Generator (RPG) cable from the PC board on the keyboard assembly.
11. Separate the PC board, keypad, and keyboard panel/label.

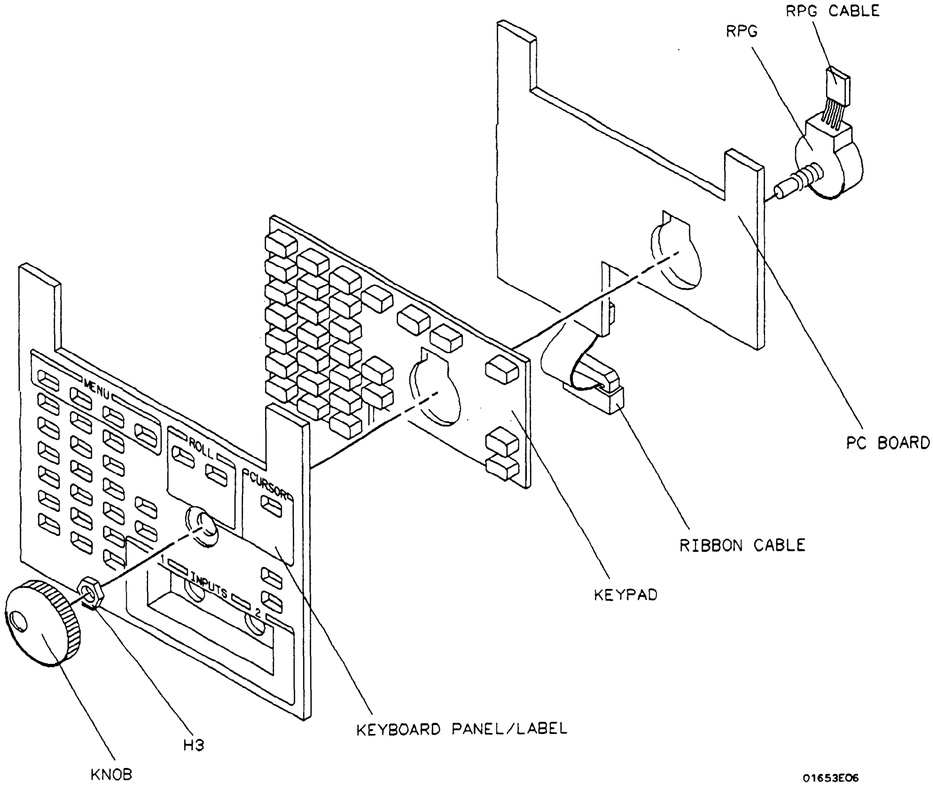
RPG CABLE
RPG
PC BOARD
RIBBON CABLE
KEYPAD
KEYBOARD PANEL/LABEL
H3
KNOB
MENU
ROLL
CURSOR
INPUTS
1
2
01653E06

Figure 6D-5. Exploded view of the Keyboard Assembly

12. The knob is force fitted on the RPG shaft. To remove the knob, pull it straight off.
13. Remove the 3/8-inch nut from the RPG.
14. Remove the RPG from the keyboard panel.
15. The keyboard label uses a self-stick adhesive. If the label must be removed, carefully peel it off.
16. Replace the keyboard assembly by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the Fan

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Rear Panel Assembly.
5. Pull the rear panel out until the fan clears the instrument cabinet. It is not necessary to completely remove the rear panel.
6. For reassembly, note the orientation of the fan cable. Remove the fan by removing the four screws securing the fan to the rear panel.
7. Replace the fan by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the Main Assembly

Caution

ELECTROSTATIC DISCHARGE can damage electronic components. Use grounded wriststraps and mats when servicing the main assembly.

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Disk Drive, Power Supply, and Oscilloscope Assembly.
5. Loosen the two screws that hold the rear bracket on the oscilloscope assembly support panel until the bracket moves freely.
6. Remove the support panel by tilting the rear of the panel up and lifting the panel out through the top of the instrument cabinet as in the previous figure 6D-4. Make sure the metal tabs on the support panel clear the front panel.
7. Remove the Rear Panel Assembly.

8. Remove the following cables from the main assembly board:
   - Disk drive cable.
   - Oscilloscope board cable.
   - Power supply cable.
   - CRT sweep cable.
   - HP-IB cable.
9. Disconnect the keyboard assembly ribbon cable from the Main Assembly.
10. Carefully place the instrument on its side.
11. From the bottom of the instrument, remove the eight screws that secure the Main Assembly to the instrument cabinet.
12. Set the instrument in the normal position.
13. Slide the main assembly out of the rear of the instrument cabinet.
14. Replace the Main Assembly by reversing this procedure.

Note

When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the CRT Monitor Assembly

The sweep board, CRT, and CRT yoke are all parts of one HP part number. They have been adjusted as a unit and should be replaced as a unit, rather than individually. Do not remove the yoke from the CRT.

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Rear Panel, Power Supply, and Main Assembly.

Caution

Discharge the post accelerator lead to the CRT monitoring band only. Components will be damaged if the post accelerator is discharged to other areas.

5. Connect a jumper lead between the mounting band of the CRT and the shaft of a screwdriver.
6. Discharge the CRT by placing the grounded screwdriver under the protective rubber cap of the post accelerator lead and momentarily touching the screwdriver to the metal clip of the post accelerator.

Caution

The CRT may charge up by itself even while disconnected. Discharge the CRT before handling. Use a jumper lead to short the CRT post accelerator terminal to the CRT mounting band.

7. Disconnect the post accelerator lead from the CRT by firmly squeezing the rubber cap until the metal clip disengages from the CRT.
8. Disconnect the following cables at the sweep board or CRT:
   - Intensity cable.
   - CRT Monitor ribbon cable.
   - Two CRT yoke cables.
   - CRT base cable.
9. Slide the sweep board up and out of the cabinet slot. When installing the sweep board, it may be necessary to press on the center of the outer shield of the sweep board to allow the board to clear the cabinet support rib.
10. Carefully place the instrument with the front panel facing down.
11. Remove the four nuts securing the CRT to the front panel.
12. Remove the sweep board guide.
13. Remove the CRT. When reinstalling the CRT, place it with the post accelerator terminal toward the inside of the instrument, away from the sweep board.
14. Replace the CRT Monitor Assembly by reversing this procedure.

Note If necessary, after replacing the CRT Monitor Assembly perform the CRT Monitor Assembly Adjustment procedures in section 4 of this manual.

Note When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

Removal and Replacement of the Feet/Tilt Stand

When necessary, refer to other removal procedures.

1. Turn off the instrument and disconnect the power cable.
2. Remove the six screws from the top and the two screws from each side of the instrument's top cover.
3. Lift off the top cover.
4. Remove the Rear Panel, Power Supply, Main Assembly, and CRT Monitor Assembly.
5. Remove the three screws securing each foot/tilt stand to the bottom of the instrument cabinet.
6. Replace the feet/tilt stand by reversing this procedure.

Note When you reinstall the top cover, insert the four screws on the sides of the cover first while making sure the cover fits into the grooves of the instrument cabinet. Then insert the six screws in the top of the cover.

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Logic Analyzers
Service Manual